CKS32F103x8
CKS32F103xB

32 Based bit ARM The core of the band 64 or 128K Byte Flash standard microcontrollers

Features

■ **Kernel: ARM32 Place Cortex ™ -M3 Kernel**

- highest 72MHz The operating frequency, in the memory 0 Waiting period access

  When up 1.25DMips / MHz (Dhrystone2.1)

- Single-cycle multiply and divide hardware

■ **Memory**

- 64KB or 128KB program Flash

- 20KB SRAM

■ **Clock, Reset and Power Management**

- 2.0 ~ 3.6 Volt power supply and I / O Pin

- Power on / off reset (POR / PDR) Programmable voltage monitor

  (PVD)

- 4 ~ 16MHz Crystal Oscillator

- Built by the factory tuned 8MHz High-speed RC Oscillator

- Embedded with calibration 40kHz Low speed RC Oscillator

- produce CPU Clock PLL

- With calibration function 32kHz RTC Oscillator

■ **2 More 12 Place ADC , 1μs Conversion time (up to 16 Input channels)**

- Conversion range: 0 to 3.6V

- Dual sample and hold function

- Temperature Sensor

■ **DMA :**

- 7 aisle DMA Controller

- Supported peripherals: timers, ADC , SPI , I_2C with USART

■ **Low power consumption**

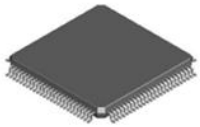
- Sleep, shutdown and standby modes

- V_{BAT} for RTC Power supply and backup registers

QFN36 6 x 6 mm

LQFP48 7 x 7 mm

LQFP64 10 x 10 mm



LQFP100 14 x 14 mm

■ Up to 80 Fast I / O port

- 26/37/51/80 More I / O Mouth, all I / O Port can be mapped to 16 A foreign

  Ministry of interruption; can withstand almost all ports 5V signal

■ **Debug mode**

- Serial wire debug (SWD) with JTAG interface

■ **7 Timers**

- 3 More 16 Bit timers, each timer with up to 4 Inputs for

  Capture / output compare / PWM And a pulse count or incremental encoder input

  channel

- 1 More 16 Bit dead-time control and emergency brake, for motor control

  PWM Advanced control timer

- 2 A watchdog timer (separate window and type)

- System timer: twenty four Decrement the bit counter type

■ **Up to 9 Communication interfaces**

- Up to 2 More I_2C Interface (support SMBus / PMBus)

- Up to 3 More USART Interface (support ISO7816 interface, LIN ,

  IrDA An interface and modem control)

- Up to 2 More SPI interface(18M Bit / sec)

- CAN interface(2.0B initiative)

- USB 2.0 Full speed interface

■ **CRC Calculation means, 96 Bit unique identification code chip**

Device Comparison

CKS32F103x8 (B) Product features and peripheral configuration

Model / peripheral interface		CKS32F103C8 / CB		CKS32F103RB	CKS32F103VB
Flash - K byte		64	128	128	128
SRAM- K byte		20		20	20
Timer	General purpose	3		3	3
	Advanced Control	1		1	1
Communication Interface	SPI	2		2	2
	I2C	2		2	2
	USART	3		3	3
	USB	1		1	1
	CAN	1		1	1
GPIO Ports (channels)		37		51	80
12 Bit synchronization ADC (Number of channels)		2 10 channels		2 16 channels	2 16 channels
CPU frequency		72 MHz			
Operating Voltage		2.0V ~ 3.6V			
Operating temperature		Ambient temperature: - 40 ℃ ~ + 85 ℃ / - 40 ℃ ~ + 105 ℃ Junction Temperature: - 40 ℃ ~ + 125 ℃			
Package		LQFP48		LQFP64	LQFP100

Ordering Information

Palletized

Product number	Package	Packed pans number	plate		Box number	Box boxing	Number of boxes loaded
CKS32F103C8T6	LQFP48	250PCS / plate	10 Tray / box	2500PCS / box		6 Box / carton	15000PCS / box
CKS32F103CBT6	LQFP48	250 PCS / plate	10 Tray / box	2500PCS / box		6 Box / carton	15000 PCS / box
CKS32F103RBT6	LQFP64	160 PCS / plate	10 Tray / box	1600 PCS / box		6 Box / carton	9600 PCS / box
CKS32F103VBT6	LQFP100	90 PCS / plate	10 Tray / box	900 PCS / box		6 Box / carton	5400 PCS / box

table of Contents

1 . Introduction

In this paper, in the core subjects CKS32F103x8 with CKS32F103xB Standard MCU Device characteristics of the product.

CKS32F103x8 with CKS32F103xB Data sheet, must be combined with its associated reference manual reading together. related Cortex ™ -M3 The core of the relevant information, please refer to " Cortex-M3 Technical Reference Manual, "available at ARM The company's website:

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/ .

2. Specifications

CKS32F103x8 with CKS32F103xB Standard MCU Series of high-performance ARM® Cortex ™ -M3 32 Bit RISC Core operating frequency is 72MHz Built-in high-speed memory (up to 128K Bytes of flash memory and 20K Byte SRAM) Rich enhancements I / O And coupled to the two ports APB Bus peripherals. Contains 2 More 12 Place ADC , 3 General purpose 16 Bit timers and 1 More PWM Timer It also includes standard and advanced communication interfaces: up to 2 More I_2C Interface and SPI interface, 3 More USART interface, 1 More USB Interface and

1 More CAN interface.

CKS32F103x8 with CKS32F103xB Standard MCU Series supply voltage 2.0V to 3.6V, -40 ° C To + 85 ° C Operating temperature range and - 40 ° C To + 105 ° C The extended temperature range, a series of power-saving mode to ensure the required low-power applications.

CKS32F103x8 with CKS32F103xB Standard products include series from 36 Foot to 100 The foot 4 Different kinds of packages; depending on the package, the peripheral configuration of the device vary. The following gives a basic introduction to the series in all peripherals.

These rich peripheral configuration such that CKS32F103x8 with CKS32F103xB Standard Series microcontrollers can be used in a variety of applications:

- Motor drive and application control
- Medical and handheld devices
- PC And gaming peripherals GPS platform
- Industrial applications: programmable logic controller (PLC) , Converter, printer and scanner
- Alarm systems, video intercom and heating, ventilation and air conditioning systems

2.1 Outline

2.1.1 ARM® of Cortex ™ -M3 The core and embedded flash memory and SRAM

ARM of Cortex ™ -M3 The processor is the latest generation of embedded ARM Processor, it is realized MCU The need to provide a low-cost platform, reduced pin count and reduced system power consumption, while delivering superior computing performance and advanced interrupt system response.

ARM of Cortex ™ -M3 Yes 32 Bit RISC Processor, provides additional code efficiency, typically in the 8 with 16 We played a bit of space on the storage system ARM Core performance.

CKS32F103x8 with CKS32F103xB Standard series has a built-in ARM Core, so it is with all the ARM Tools and software compatibility. **Error! Unrecognizable switching parameter.** A functional block diagram of the series.

2.1.2 Built-in flash memory

64K or 128K Bytes of built-in flash memory for storing programs and data.

2.1.3 CRC (Cyclic Redundancy Check) calculation unit

CRC (Cyclic Redundancy Check) calculation unit uses a fixed generator polynomial from a 32 Generating a bit data word CRC code. In many applications, based on CRC Techniques are used to verify the consistency of the data transmission or storage. in EN / IEC 60335-1 The range of the standard, which provides a means of detecting errors of a flash memory, CRC The software calculating unit may calculate in real time for the signature, and the signature generated in comparison with the link and to generate a software.

2.1.4 Internal SRAM

20K Built-in bytes SRAM , CPU Able to 0 Waiting period to access (read / write).

2.1.5 Nested vectored interrupt controller (NVIC)

CKS32F103x8 with CKS32F103xB Standard built-nested vectored interrupt controller that can handle up to 43 Maskable interrupt channels (not including 16 More Cortex ™ -M3 The break) and 16 Priority levels.

- Tightly coupled NVIC It can achieve low latency interrupt handling
- Interrupt vector entry address directly into the kernel
- Tightly coupled NVIC interface
- Allow early treatment interruption
- Late arrival of a higher priority process interrupt
- Link function supports interrupt Tail
- Processor state automatically saved
- Automatic recovery upon return, at no additional cost to the command module with

minimal disruption delay in providing flexible interrupt management functions.

2.1.6 External Interrupt / Event Controller (EXTI)

External Interrupt / Event Controller included 19 An edge detector, for generating an interrupt / event request. Each interrupt may be independently configure its trigger event (rising or falling edge or both edges), and can be individually shielded; a pending register maintained by the status of all interrupt requests. EXTI Less than the internal width can be detected APB2 Pulse of the clock period. Up to 80 General purpose I / O Port is connected to 16 External interrupt lines.

2.1.7 Clock and start

The system clock is carried out at startup, the internal reset 8MHz of RC Oscillator is selected as the default CPU Clock, can then select the exterior and having a failure detection 4 ~ 16MHz Clock; the external clock when the failure is detected, it will be isolated, the system will automatically switch to the internal RC Oscillator, if the interrupt is enabled, the software may receive a corresponding interrupt. Similarly, when necessary, to take PLL Clock completely

Interrupt management (such as when using the external oscillator during a failure).

Prescaler for configuring a plurality of AHB Frequency, high-speed APB (APB2) And low-speed APB (APB1) region. AHB And high-speed APB The highest frequency is 72MHz Low speed APB The highest frequency of 36MHz . Reference FIG. 2 As shown in a block diagram of a driving clock.

2.1.8 Bootstrap mode

At startup, the bootstrap pin by a self-lifting choice of three modes:

- Bootstrap program from the flash memory
- Bootstrap from the system memory
- From the inside SRAM Bootstrap bootstrap loader (Bootloader) Stored in the system memory, through USART1 Flash reprogramming.

2.1.9 Supply Scheme

- V_{DD} = 2.0 ~ 3.6V : V_{DD} Pin I / O Pin and the internal power supply voltage regulator.
- V_{SSA} , V_{DDA} = 2.0 ~ 3.6V :for ADC , Reset module, RC And oscillator PLL The analog section provides power. use ADC Time, V_{DDA} Not less than 2.4V . V_{DDA} with V_{SSA} It must be connected respectively to V_{DD} with V_{SS} .
- V_{BAT} = 1.8 ~ 3.6V : When you close V_{DD} When (the internal power source through the switch) of RTC ,external 32kHz Power oscillator and backup registers.

For more information on how to connect the power pins, see FIG. 10 Supply Scheme.

2.1.10 Power Monitor

This product incorporates an internal power-on reset (POR) / Brown-out reset (PDR) Circuit, the circuit is always active to ensure power supply system in more than 2V Work; when V_{DD} Below the set threshold ($V_{POR/PDR}$) When the device is set to the reset state, without having to use an external reset circuit. There is also a programmable device voltage monitor (PVD) That monitors V_{DD} / V_{DDA} Power supply and with the threshold V_{PVD} Comparison, when V_{DD} Below or above the threshold V_{PVD}
When an interrupt, the interrupt handler can issue a warning or a microcontroller into a safe mode. PVD Function need to open a program. on $V_{POR/PDR}$ with V_{PVD} Value reference table 8 .

2.1.11 Regulator

The regulator has three operating modes: master mode (MR) Low-power mode (LPR) And a shutdown mode

- Master mode (MR) Operation for normal operation
- Low-power mode (LPR) For CPU Shutdown mode
- Shutdown mode for CPU Standby mode: the output of the regulator is high impedance state, the core power supply circuit is cut, consumption state at zero voltage regulator (but registers and SRAM The contents will be lost)

The regulator after reset is always active, closed in standby mode in a high impedance output.

2.1.12 Low-power mode

CKS32F103x8 with CKS32F103xB Standard product supports three low-power modes, you can achieve the best balance between the requirements of low-power, short start-up time and a variety of wake-up events.

- **Sleep Mode**

In sleep mode, only MCU Stop, all peripherals can wake up in a working state in the event of interruption / event MCU .

- **Shutdown Mode**

In keeping SRAM And the case where the register contents are not lost, shutdown mode may achieve the lowest power consumption. In shutdown mode, stop all internal 1.5V Part of the power supply, PLL , HSI of RC And oscillator HSE The crystal oscillator is turned off, the regulator may be placed in the normal mode or the low power mode.

Can be configured by any of a EXTI A signal to wake up the microcontroller from the shutdown mode, EXTI Signal can be 16 External I / O One of mouth, PVD Output, RTC Alarm clock or USB The wake-up signal.

- **Standby mode**

In the standby mode you can achieve the lowest power consumption. The internal voltage regulator is turned off, and therefore all internal 1.5V The power supply portion is cut off; PLL , HSI of RC And oscillator HSE The crystal oscillator is also turned off; into standby mode, SRAM And register content will disappear, but the contents of the register remain a backup, standby circuit still work.

Exit from standby mode conditions are: NRST The external reset signal, IWDG Reset WKUP A pin on the rising edge or RTC When the alarm occurs.

NOTE: When entering the stop or standby mode, RTC , IWDG And the corresponding clock is not stopped.

2.1.13 DMA

flexible 7 General road DMA You can manage memory to memory, and the memory device to the memory to the data transmission device; DMA The controller supports the ring buffer management, interrupt controller to avoid the transmission reaches the end of the buffer generated.

Each channel has a dedicated hardware DMA Request logic, and each channel can be triggered by software; source and destination addresses of the length of the transmission, the transmission can be set independently by software.

DMA The main peripherals can be used: SPI , I_2C , USART And general, basic and advanced control timer TIMx with ADC .

2.1.14 RTC (Real-time clock) and backup registers

RTC And backup power supply through a switch registers, in V_{DD} When the switch selects the active V_{DD} Otherwise, the V_{BAT} Pin power supply. Backup registers (10 More 16 Bit registers) can be used in a closed V_{DD} When, save 20 User application data bytes. RTC And backup registers are not reset the system reset or power source; when waking from standby mode, will not be reset.

Real-time clock counter with a set of continuous operation, calendar clock function can be provided by appropriate software, also has alarm interrupt and periodic interrupt function. RTC A clock driver may use external crystal 32.768kHz Oscillator, low power internal RC Oscillator or an external clock by a high speed 128 Divider. Internal low-power RC A typical oscillator frequency 40kHz . To compensate for the deviation of the natural lens, can output a 512Hz The signal RTC Clock calibration. RTC Have a 32 Bit programmable counter, the comparison registers

To be measured over time. There is a 20 Bit prescaler for time base clock, the clock for the default 32.768kHz , It will generate a 1 Seconds long time base.

2.1.15 And Watchdog Timer

CKS32F103x8 with CKS32F103xB Standard products include 1 An advanced control timers, 3 General timer, and 2 And a watchdog timer 1 A system timer.

The following table compares the functionality of advanced control timers, general timer and basic timers:

table 1 Timer feature comparison

Timer Counter resolution Counter Type Generating prescaler DMA please				begging	Capture / compare channels complementary output	
TIM1	16 Place	Up-counting / down-counting	1 ~ 65536 Any integer between	can	4	Have
TIM2 TIM3 TIM4	16 Place	Up-counting / down-counting	1 ~ 65536 Any integer between	can	4	No

Advanced control timer (TIM1)

Advanced control timer (TIM1) It can be seen to be assigned 6 Three-phase channels PWM Generator, having a complementary dead band inserted PWM Output can also be treated as a complete general-purpose timer. 4 Independent channels can be used:

- Input Capture
- Output Compare
- produce PWM (Edge or center aligned mode)
- Configured to output a single pulse 16 When the bit standard timers, it TIMx Timers have the same functionality. Configured to 16 Place PWM When the generator having a full modulation capability (0 to 100%) .

In debug mode, the counter can be frozen, while PWM Output is disabled, thereby disconnecting switch controlled by the output of these. Many features are standard TIM Same timer, the internal structure is the same, so the advanced control timer via the timer function and links TIM Timer co-operation, providing synchronous or event link function.

General-purpose timers (TIMx)

CKS32F103x8 with CKS32F103xB Standard products, built up to 3 A standard timer can be run simultaneously (TIM2 , TIM3 with TIM4) . Each timer has a 16 Incrementing bit automatic loading / down counter, a 16 Bit prescaler and 4 Independent channels, each channel can be used as input capture, output compare, PWM And a one-pulse mode output, the maximum package configuration can provide up to 12 Input capture, output compare or PWM aisle.

They can also work together by linking a timer function and advanced control timers, providing synchronous or event link function. In debug mode, the counter can be frozen. Any standard timer can be used to generate PWM Output. Each timer has independent DMA Request mechanism.

These timers also capable of processing signals of the incremental encoder, can handle 1 to 3 A digital output Hall sensor.

Independent watchdog

Independent watchdog is based on a 12 Bit down counter and a 8 Bit prescaler, which consists of a separate internal 40kHz of RC A clock oscillator; for this RC Independent of the master clock oscillator, it can operate in shutdown mode and a standby mode. It can be used as a watchdog reset the entire system when a problem occurs, or as a time-out timer provides free management application. It can be configured by the option byte to start a software or hardware watchdog. In debug mode, the counter can be frozen.

Window Watchdog

Window contains a watchdog 7 Bits can be configured as free-running down counter. When used as a watchdog, reset the entire system if a problem occurs. It is driven by the master clock, having an early warning interrupt function; in debug mode, the counter can be frozen.

Timer-based system

This timer can be dedicated to real-time operating system, it can use as a standard down counter. It has the following characteristics:

- twenty four Bit down counter
- Auto reload function
- When the counter 0 When the system generates a maskable interrupt
- Programmable clock source

2.1.16 I2C bus

Up to 2 More I₂C Bus interface that operates in multi-master mode or slave mode, supports standard mode and fast mode.

I₂C Interface Support 7 Position or 10 Bit addressing, 7 Bit address from the dual mode addressing. Built-in hardware CRC Generator / checker. The interface can be used DMA Operation and Support SMBus bus 2.0 Version/ PMBus bus.

2.1.17 Universal Synchronous / Asynchronous Receiver Transmitter (USART)

USART1 Interface communication speed up 4.5Mb / s Other interface communication speed up Mb / s . USART Interfaces with hardware CTS with RTS Signal management, support IrDA SIR ENDEC Transmission codec compatible ISO7816 Smart cards and provide LIN Master / slave function.

all USART Interface can be used DMA operating.

2.1.18 Serial Peripheral Interface (SPI)

Up to 2 More SPI Interface may be configured to communicate reachable from master mode or rate mode, half-duplex and full-duplex 18 Mb / s . 3 Generating bit prescaler 8 Species main mode frequency, may be configured to 8 Position or 16 Bit data frame format. hardware CRC Generation / verification support basic SD Card and MMC mode.

all SPI Interface can be used DMA operating.

2.1.19 Controller Area Network (CAN)

CAN Interface specification compatible 2.0A with 2.0B (Initiative), bit rate up 1 Mb / s . It can receive and send 11 Standard frame bit identifier may be transmitted and received 29 Extended frame bit identifier. have 3 E-mail and transmit 2 Receive FIFO , 3 level 14 An adjustable filter.

2.1.20 Universal Serial Bus (USB)

CKS32F103x8 with CKS32F103xB Standard products, built a full-speed compatible USB The device controller, follow full speed USB device(12 Mb / s) Standard, the endpoint may be a software configuration, having a standby / wake-up function. USB Dedicated 48MHz Internal master clock PLL Produced directly (the clock source must be a HSE Crystal Oscillator).

2.1.21 GPIO ports (GPIO)

Each GPIO Pins can be configured by software to output (open-drain or push-pull), input (pull-down or pull-up or floating) or peripheral functions of the port. most GPIO Pins are shared with multiplexed analog or digital peripherals. In addition to having an analog input, all GPIO Pins allow a large current.

In case of need, I / O Pin through a specific peripheral function lock operation, to avoid I / O Unexpected register write operation. in APB2 Up I / O Flip up the foot speed 18MHz .

2.1.22 ADC (An analog / digital converter)

CKS32F103x8 with CKS32F103xB Embedded Standard Products 2 More 12 Bit analog / digital converter (ADC) Each ADC Share up to 16 External channels, enabling a single conversion or scan conversion mode. In scan mode, it can be switched on automatically in a selected group of analog input pins.

ADC Other logic functions on the interface comprising:

- Synchronous sample and hold
- CROSS sample and hold
- A single sample

ADC can use DMA operating.

The watchdog can be very accurately simulate the way monitoring, multiple or all of the selected channel, when the monitored signal exceeds the preset threshold, the analog watchdog interrupt is generated.

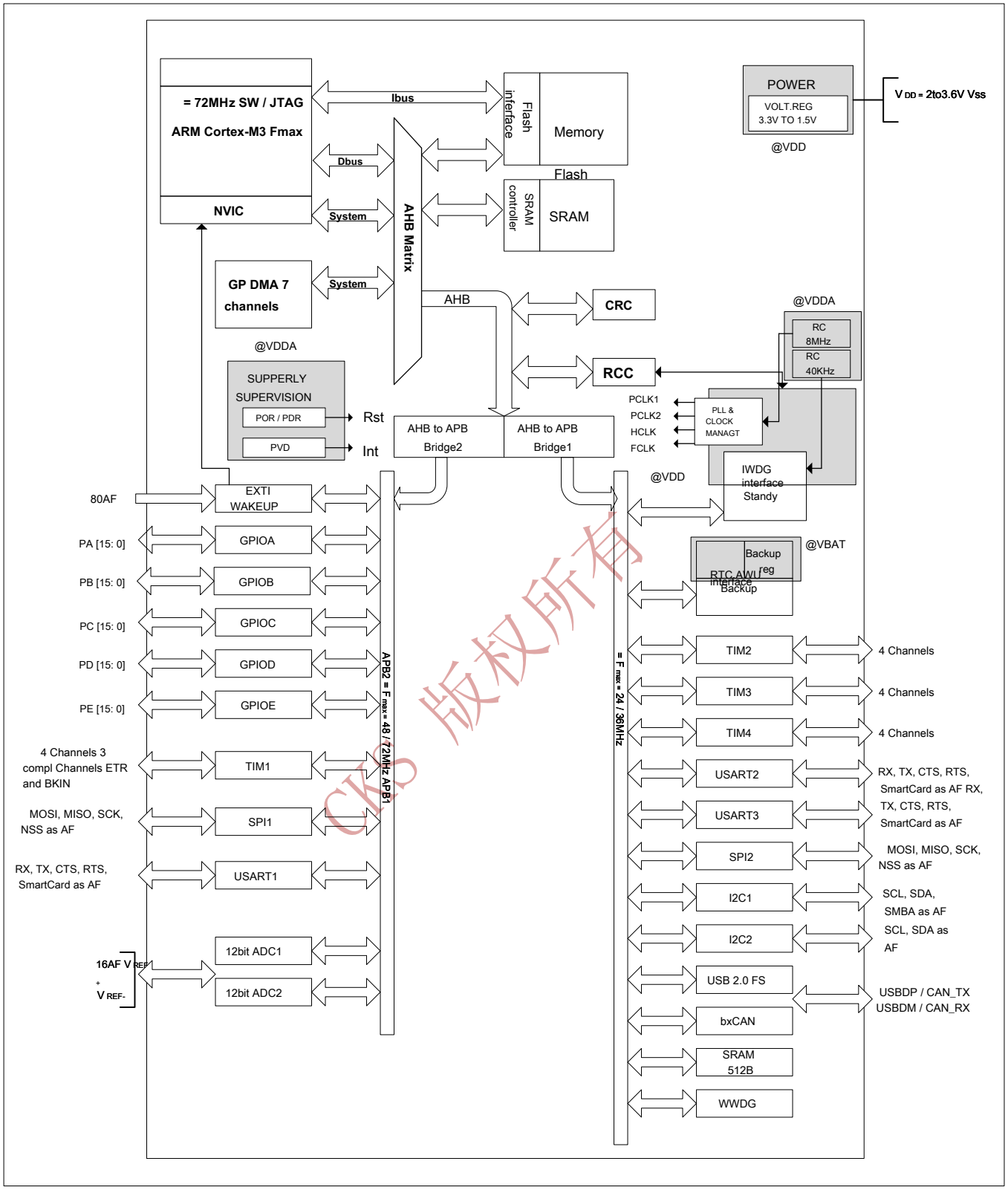
By the standard Timer (TIMx) And advanced control timer (TIM1) Event occurs, it is possible to cascade inside respectively ADC Trigger and trigger the beginning of the injection, the application can AD Conversion and clock synchronization.

2.1.23 Temperature Sensor

The temperature sensor generates a voltage varies linearly with temperature, in the range of conversion 2V <V_{DDA}< 3.6V between. The temperature sensor is connected to the inside ADC12_IN16 The input channel, for converting the sensor output to a digital value.

2.1.24 Serial wire JTAG Debug port (SWJ-DP)

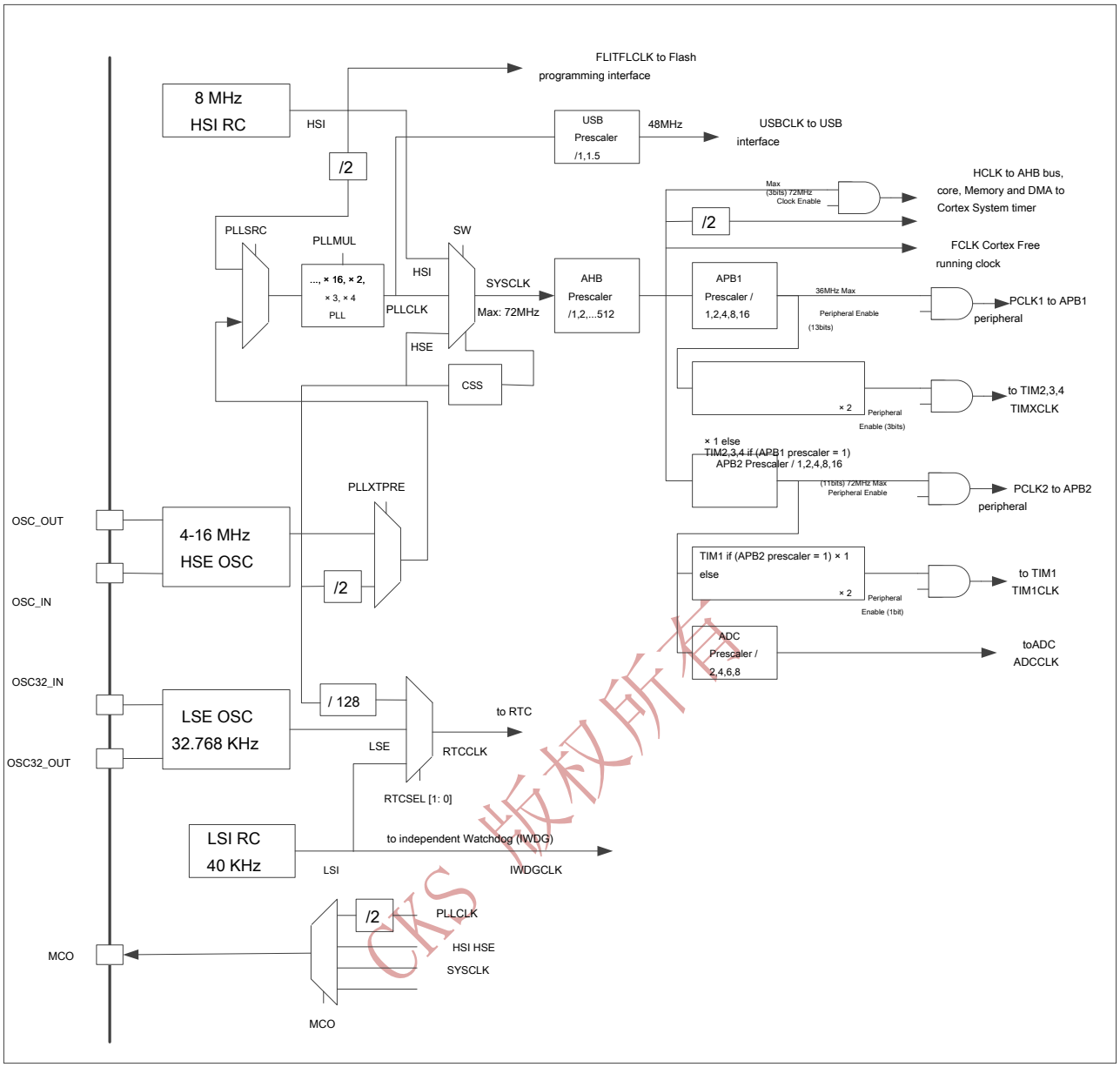
Embedded ARM of SWJ-DP Interface, which is a combination of JTAG And serial wire debug interface, serial wire debug interface or JTAG Connection interface. JTAG of TMS with TCK Signals and SWDIO with SWCLK Common pin, TMS A particular signal sequence for feet JTAG-DP with SW-DP Switch between.



Map 1 System block diagram

1. Operating temperature:- 40 ° C To + 105 ° C , The junction temperature of 125 ° C .

2. AF : As a peripheral functions of the foot I / O port



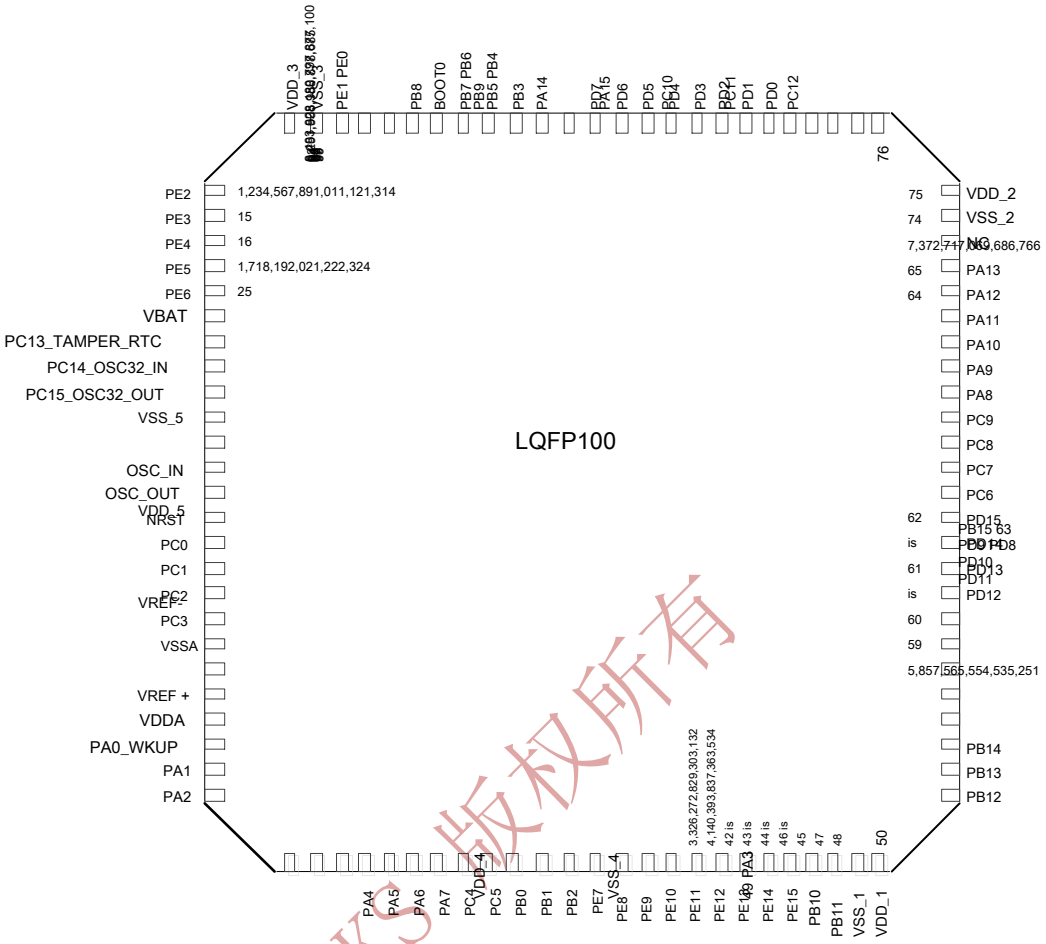
Map 2 Clock tree

1 . when HSI As a PLL When the input clock, the maximum clock frequency of the system can only reach 64MHz .

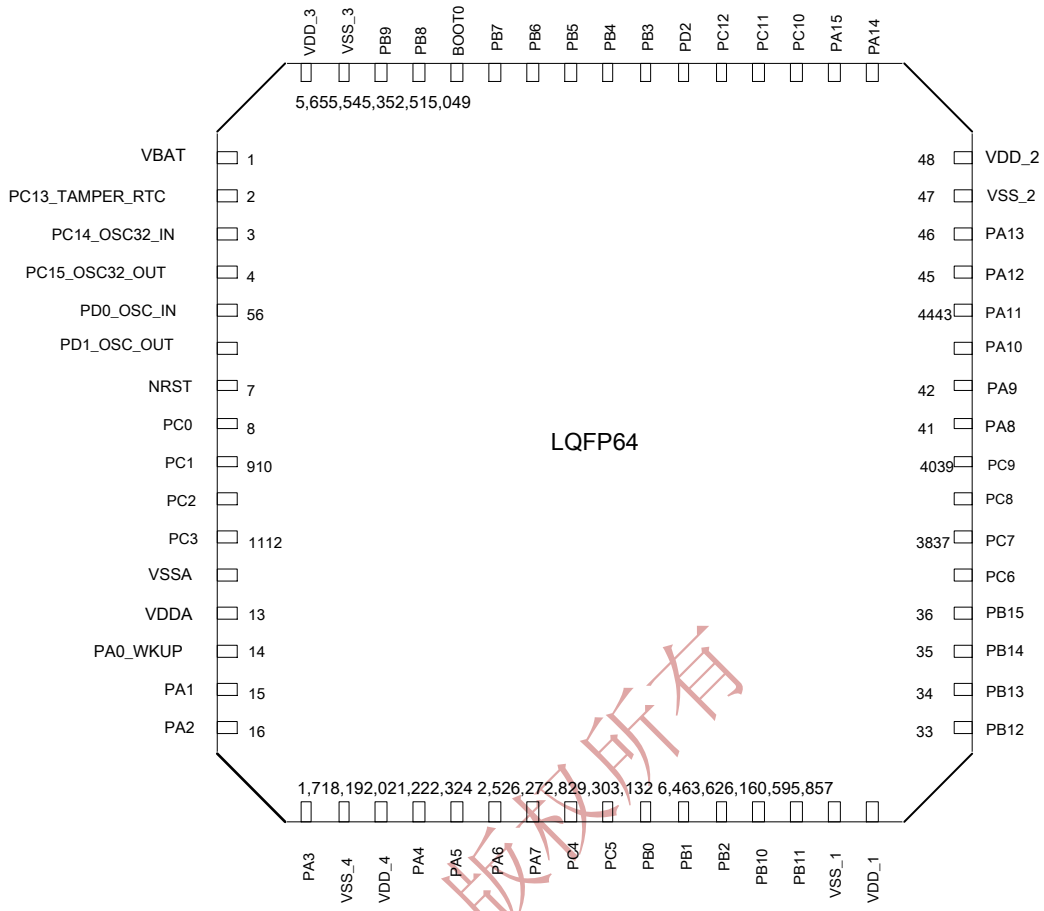
2 . When USB When the function, you must also use HSE with PLL , CPU The frequency must be 48MHz or 72MHz .

3 . When you need ADC Sampling time 1μs Time, APB2 Must be set 14MHz , 28MHz or 56MHz .

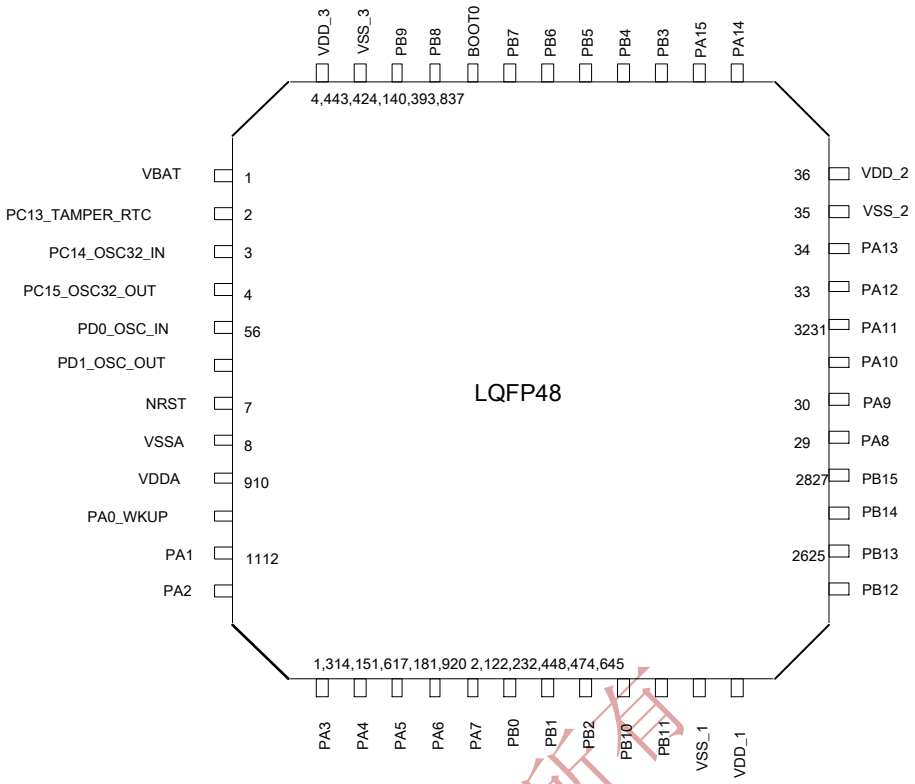
3. Pin definitions



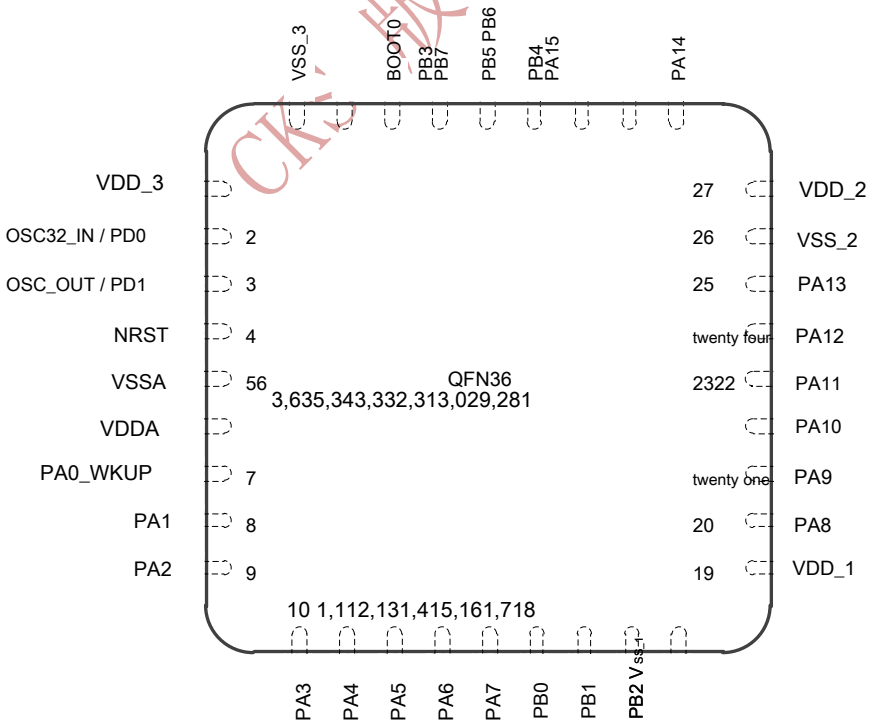
Map 3CKS32F103xx Standard LQFP100 Pinout



Map 4CKS32F103xx Standard LQFP64 Pinout



Map 5CKS32F103xx Standard LQFP48 Pinout



Map 6CKS32F103xx Standard QFN36 Pinout

table 2CK S 32F10 3xx Pin definitions

Pin Number				Pin name of the class	Electrically (1)	I / O level (2)	Main features (3) (Reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
-	-	1	-	PE2	I / O FT		PE2	TRACECK	
-	-	2	-	PE3	I / O FT		PE3	TRACED0	
-	-	3	-	PE4	I / O FT		PE4	TRACED1	
-	-	4	-	PE5	I / O FT		PE5	TRACED2	
-	-	5	-	PE6	I / O FT		PE6	TRACED3	
1	1	6	-	V_{BAT}	S		V_{BAT}		
2	2	7	-	PC13-TAMPER-RTC (4)	I / O		PC13	TAMPER-RTC	
3	3	8	-	PC14-OSC32_IN (4)	I / O		PC14	OSC32_IN	
4	4	9	-	PC15-OSC32_OUT (4)	I / O		PC15	OSC32_OUT	
-	-	10	-	V_{SS_5}	S		V_{SS_5}		
-	-	11	-	V_{DD_5}	S		V_{DD_5}		
5	5	12	2	OSC_IN	I		OCS_IN		PD0 (7)
6	6	13	3	OSC_OUT	O		OSC_OUT		PD1 (7)
7	7	14	4	NRST	I / O		NRST		
-	8	15	-	PC0	I / O		PC0	ADC12_IN10	
-	9	16	-	PC1	I / O		PC1	ADC12_IN11	
-	10	17	-	PC2	I / O		PC2	ADC12_IN12	
-	11	18	-	PC3	I / O		PC3	ADC12_IN13	
8	12	19	5	V_{SSA}	S		V_{SSA}		
-	-	20	-	V_{REF-}	S		V_{REF-}		
-	-	twenty one	-	V_{REF+}	S		V_{REF+}		
9	13	twenty two	6	V_{DDA}	S		V_{DDA}		
10	14	twenty three	7	PA0-WKUP	I / O		PA0	WKUP / USART2_CTS (6) / ADC12_IN0 / TIM2_CH1_ETR (6)	
11	15	twenty four	8	PA1	I / O		PA1	USART2_RTS (6) / ADC12_IN1 / TIM2_CH2 (6)	
12	16	25	9	PA2	I / O		PA2	USART2_TX (6) / ADC12_IN2 / TIM2_CH3 (6)	
13	17	26	10	PA3	I / O		PA3	USART2_RX (6) / ADC12_IN3 / TIM2_CH	

Pin Number				Pin name of the class	Electrically (1)	I / O level (2)	Main features (3) (Reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
								4 (6)	
-	18	27	-	V_{SS_4}	S		V_{SS_4}		
-	19	28	-	V_{DD_4}	S		V_{DD_4}		
14	20	29	11	PA4	I / O		PA4	SPI1_NSS (6) / USART2_CK (6) / ADC12_IN4	
15	twenty one	30	12	PA5	I / O		PA5	SPI1_SCK (6) / ADC12_IN5	
16	twenty two	31	13	PA6	I / O		PA6	SPI1_MISO (6) / ADC12_IN6 / TIM3_CH1 (6)	TIM1_BKIN
17	twenty three	32	14	PA7	I / O		PA7	SPI1_MOSI (6) / ADC12_IN7 / TIM3_CH2 (6)	TIMI_CHIN
-	twenty four	33	-	PC4	I / O		PC4	ADC12_IN14	
-	25	34	-	PC5	I / O		PC5	ADC12_IN15	
18	26	35	15	PB0	I / O		PB0	ADC12_IN8 / TIM3_CH3 (6)	TIM1_CH2N
19	27	36	16	PB1	I / O		PB1	ADC12_IN9 / TIM3_CH4 (6)	TIM1_CH3N
20	28	37	17	PB2	I / O FT		PB2 / BOOT1		
-	-	38	-	PE7	I / O FT		PE7		TIM1_ETR
-	-	39	-	PE8	I / O FT		PE8		TIM1_CH1N
-	-	40	-	PE9	I / O FT		PE9		TIM1_CH1
-	-	41	-	PE10	I / O FT		PE10		TIM1_CH2N
-	-	42	-	PE11	I / O FT		PE11		TIM1_CH2
-	-	43	-	PE12	I / O FT		PE12		TIM1_CH3N
-	-	44	-	PE13	I / O FT		PE13		TIM1_CH3
-	-	45	-	PE14	I / O FT		PE14		TIM1_CH4
-	-	46	-	PE15	I / O FT		PE15		TIM1_BKIN
twenty one	29	47	-	PB10	I / O FT		PB10	I2C2_SCL / USART3_TX (6)	TIM2_CH3
twenty two	30	48	-	PB11	I / O FT		PB11	I2C2_SDA / USART3_RX (6)	TIM2_CH4
twenty three	31	49	18	V_{SS_1}	S		V_{SS_1}		
twenty four	32	50	19	V_{DD_1}	S		V_{DD_1}		

Pin Number				Pin name of the class	Electrically (1)	I / O level (2)	Main features (3) (Reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
25	33	51	-	PB12	I / O	FT	PB12	SPI2_NSS / I2C2_SMBAI / USART3_CK (6) / TIM1_BKIN (6)	
26	34	52	-	PB13	I / O	FT	PB13	SPI2_SCK / USART3_CTS (6) / TIM1_CH1N (6)	
27	35	53	-	PB14	I / O	FT	PB14	SPI2_MISO / USART3_CTS (6) / TIM1_CH2N (6)	
28	36	54	-	PB15	I / O	FT	PB15	SPI2_MOSI / TIM1_CH3N (6)	
-	-	55	-	PD8	I / O	FT	PD8		USART3_TX
-	-	56	-	PD9	I / O	FT	PD9		USART3_RX
-	-	57	-	PD10	I / O	FT	PD10		USART3_CK
-	-	58	-	PD11	I / O	FT	PD11		USART3_CTS
-	-	59	-	PD12	I / O	FT	PD12		TIM4_CH1 / USART3_RTS
-	-	60	-	PD13	I / O	FT	PD13		TIM4_CH2
-	-	61	-	PD14	I / O	FT	PD14		TIM4_CH3
-	-	62	-	PD15	I / O	FT	PD15		TIM4_CH4
-	37	63	-	PC6	I / O	FT	PC6		TIM3_CH1
-	38	64	-	PC7	I / O	FT	PC7		TIM3_CH2
-	39	65	-	PC8	I / O	FT	PC8		TIM3_CH3
-	40	66	-	PC9	I / O	FT	PC9		TIM3_CH4
29	41	67	20	PA8	I / O	FT	PA8	USART1_CK / TIM1_CH1 (6) / MCO	
30	42	68	twenty one	PA9	I / O	FT	PA9	USART1_TX (6) / TIM1_CH2 (6)	
31	43	69	twenty two	PA10	I / O	FT	PA10	USART1_RX (6) / TIM1_CH3 (6)	
32	44	70	twenty three	PA11	I / O	FT	PA11	USART1_CTS / USBDM / CANRX (6) / TIM1_CH4 (6)	
33	45	71	twenty four	PA12	I / O	FT	PA12	USART1_RTS / USBDP / CANTX (6) / TIM1_ETR (6)	

Pin Number				Pin name of the class	Electrically (1)	I / O level (2)	Main features (3) (Reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
34	46	72	25	PA13	I / O	FT	JTMS / SWD IO		PA13
-	-	73	-	not connected					
35	47	74	26	V_{SS_2}	S		V_{SS_2}		
36	48	75	27	V_{DD_2}	S		V_{DD_2}		
37	49	76	28	PA14	I / O	FT	JTCK / SWCLK		PA14
38	50	77	29	PA15	I / O	FT	JTDI		TIM2_CH1_ETR PA15 / SPI1_NSS
-	51	78	-	PC10	I / O	FT	PC10		USART3_TX
-	52	79	-	PC11	I / O	FT	PC11		USART3_RX
-	53	80	-	PC12	I / O	FT	PC12		USART3_CK
		81	2	PD0	I / O	FT	OSC_IN (8)		CANRX
		82	3	PD1	I / O	FT	OSC_OUT (8)		CANTX
-	54	83	-	PD2	I / O	FT	PD2	TIM3_ETR	
-	-	84	-	PD3	I / O	FT	PD3		USART2_CTS
-	-	85	-	PD4	I / O	FT	PD4		USART2_RTS
-	-	86	-	PD5	I / O	FT	PD5		USART2_TX
-	-	87	-	PD6	I / O	FT	PD6		USART2_RX
-	-	88	-	PD7	I / O	FT	PD7		USART2_CK
39	55	89	30	PB3	I / O	FT	JTDO		PB3 / TRACESWO / TIM2_CH2 / SPI1_SCK
40	56	90	31	PB4	I / O	FT	JNTRST		PB4 / TIM3_CH1 / SPI1_MISO
41	57	91	32	PB5	I / O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
42	58	92	33	PB6	I / O	FT	PB6	I2C1_SCL (6) / TIM4_CH1 (6)	USART1_TX
43	59	93	34	PB7	I / O	FT	PB7	I2C1_SDA (6) / TIM4_CH2 (6)	USART1_RX
44	60	94	35	BOOT0	I		BOOT0		
45	61	95	-	PB8	I / O	FT	PB8	TIM4_CH3 (6)	I2C1_SCL / CANRX
46	62	96	-	P89	I / O	FT	P89	TIM4_CH4 (6)	I2C1_SDA / CANTX

Pin Number				Pin name of the class	Electrically (1)	I / O level (2)	Main features (3) (Reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
-	-	97	-	PE0	I / O FT		PE0	TIM4_ETR	
-	-	98	-	PE1	I / O FT		PE1		
47	63	99	36	V_{SS_3}	S		V_{SS_3}		
48	64	100	1	V_{DD_3}	S		V_{DD_3}		

1. I = Input, O = Output, S = power supply

2. FT : 5V Voltage tolerance

3. PC13 , PC14 with PC15 Pin power through the power switch, and this power switch can only absorb a limited current (3mA) . So these three pins as

   The following restrictions apply when output pin: Only one pin can be used as output at the same time, as an output pin can only work in 2MHz Mode, the maximum drive load

   for 30pF , And not as a current source (e.g., driver LED) .

4. These first pins in the backup area in the main menu on power state, even after the reset, the state of these pins is controlled by the backup zone register (the register

   Register will not be reset system master reset). About how to control them IO Specific information mouth, please refer to CKS32F103x8 with CKS32F103xB Reference book

   Battery backup area, and BKP Relevant sections of the register.

5. Such multiplexing function can be configured by software to the other pin (if the corresponding models this pin package), details refer to CKS32F103x8 with

   CKS32F103xB Reference Manual multiplexing function I / O Chapters and debug settings section.

6. QFN36 Pins of the package 2 And pin 3 , LQFP48 with LQFP64 Pins of the package 5 And pin 6 In the chip reset to default configuration OSC_IN with

   OSC_OUT Function foot. Software can reset these two pins PD0 with PD1 Features. But for LQFP100 Package, since PD0 with PD1 It is inherent

   Function pin, so no need to re-image set by the software. For more details, please refer to CKS32F103x8 with CKS32F103xB Reference Manual

   Alternate Function I / O Chapters and debug settings section. In the output mode, PD0 with PD1 It can only be configured 50MHz Output mode.

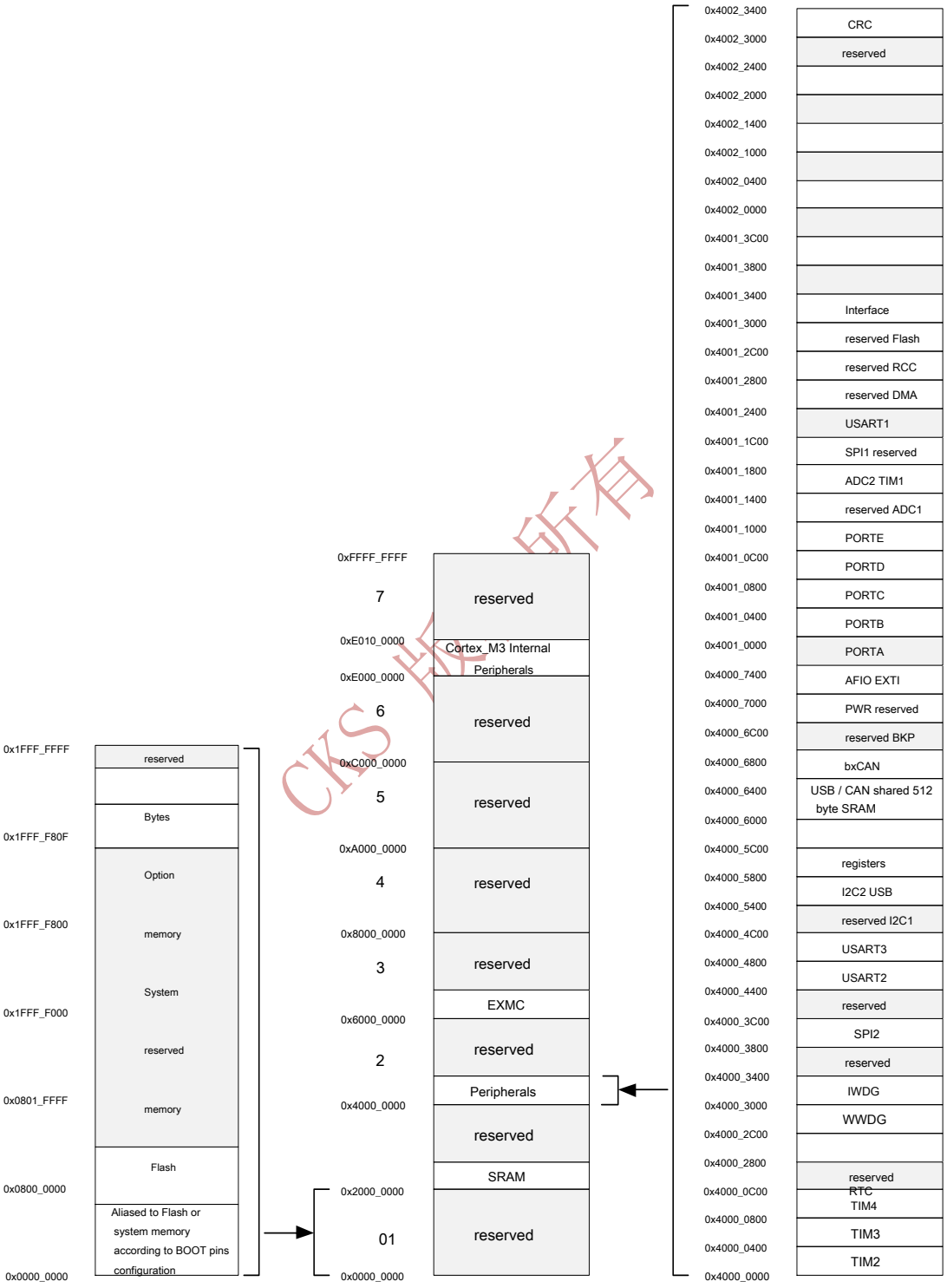
7. Mark appears in the table of pin names ADC12_INx (x Show 0 ~ 15 Integer), indicates that this pin can be ADC1_INx or ADC2_INx .

   E.g: ADC12_IN9 This pin can be configured to represent ADC1_IN9 It can also be configured to ADC2_IN9 .

8. Table Pin PA0 Corresponding to the multiplexing functions TIM2_CH1_ETR Indicating that you can configure the function TIM2_TI1 or TIM2_ETR . Similarly, PA15

   The name of the corresponding remapping multiplexing functions TIM2_CH1_ETR , It has the same meaning.

4. Memory map



Map 7 Memory MAP Map

5. Electrical Characteristics

5.1 Test Conditions

Unless otherwise specified, all voltages are to V_{SS} As a benchmark.

5.1.1 The minimum and maximum values

Unless otherwise specified, the production line by 100% Products at ambient temperature T_A = 25 ° C with T_A = T_A max Under the test performed (T_A max Matches the selected temperature range), the minimum and maximum values of all guaranteed under worst case ambient temperature, supply voltage and clock frequency.

Described in comment to each of the tables below, the analog design and / or process properties of the resulting data without test production line provides evaluation; the basis of comprehensive evaluation on the minimum and maximum values through the sample after the test, then the mean value plus or minus three times the standard distribution (average ± 3Σ) get.

5.1.2. Typical values

Unless otherwise specified, typical data are based on T_A = 25 ° C with V_{DD} = 3.3V (2V ≤ V_{DD} ≤ 3.3V voltage range). These data are only used for design guidance and are not tested.

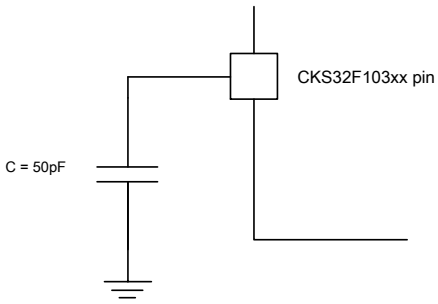
typical ADC Numerical accuracy is obtained by a batch of standard samples, obtained at all temperatures tested range, 95% Product numerical error given less (mean ± 2 Σ) .

5.1.3 Typical curve

Unless otherwise noted, typical curve for design guidance only and are not tested.

5.1.4 Load Capacitance

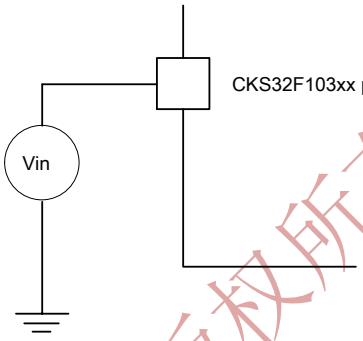
When the measured load condition parameters shown in FIG pins 8 in.



Map 8 Pin load conditions

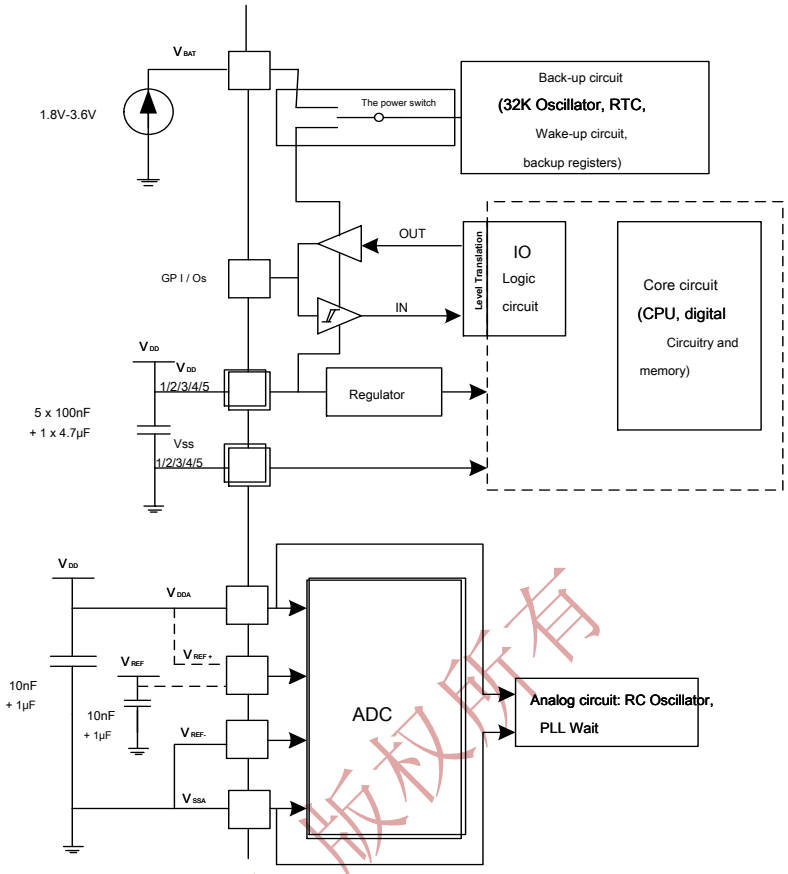
5.1.5 Pin input voltage

Measuring the input voltage on pin embodiment shown in FIG. 9 in.



Map 9 Pin input voltage

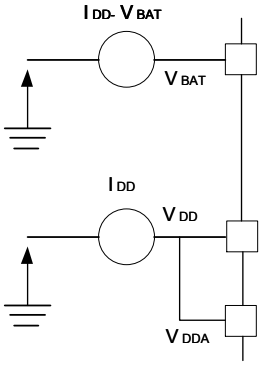
5.1.6 Supply Scheme



Map 10 Supply Scheme

Note: The image above 4.7μF Capacitor must be connected to V DD3 .

5.1.7 Current consumption measurement



Map 11 Current consumption measurement scheme

5.2 Absolute Maximum Ratings

Applied load on the device exceeds the absolute maximum rating list (table 3 ,table 4 ,table 5) The values given, may result in permanent damage to the device. Given here is able to withstand the maximum load, does not mean that the functional condition of correct operation of this device. Long-term work in the device under maximum conditions may affect device reliability.

table 3 Voltage characteristics

symbol	description	Minimum	Maximum	unit
V_{DD} - V_{SS}	External main supply voltage (comprising V_{DDA} with V_{DD}) (1)	-0.3	4.0	V
V_{IN}	in 5V The tolerance on the input voltage pin (2)	V_{SS} - 0.3	V_{DD} + 4.0	
	On the other voltage input pin (2)	V_{SS} - 0.3	4.0	
$\|\Delta V_{DDx}\|$	The voltage difference between the different supply pin		50	mV
$\|V_{SSX} - V_{SS}\|$	The voltage difference between the different ground pins		50	
$V_{ESD (HBM)}$	ESD Electrostatic discharge voltage (Human Body Model)	See 5.3.11 Festival		

1 . All the power (V_{DD}, V_{DDA}) And ground (V_{SS}, V_{SSA}) Pin must always be connected to the external power supply system within the allowed range.

2 . $I_{INJ (PIN)}$ Must not exceed its limit (see Table 4) , Which is to ensure V_{IN} Do not exceed their maximum. If you can not guarantee V_{IN} Does not exceed its maximum value, but also to ensure the External constraints $I_{INJ (PIN)}$ Do not exceed their maximum. when $V_{IN} > V_{IN}$ max When there is a positive injection current; when $V_{IN} < V_{SS}$ When there is a reverse injection current.

table 4 Current characteristics

symbol	description	Max Unit	
I_{VDD}	through V_{DD} / V_{DDA} The total current of the power supply line (supply current) (1)	150	mA
I_{VSS}	through V_{SS} The total ground current (flowing current) (1)	150	
I_{IO}	Arbitrarily I / O And sink current output on the control pin	25	
	Arbitrarily I / O And the output current of the control pin	--25	
$I_{INJ (PIN)}$ (2) (3)	5V Injection current tolerance Pin	--5 / + 0	
	Other injection current pin (4)	± 5	
$\Sigma I_{INJ (PIN)}$ (2)	all I / O And the total injection current of the control pin (4)	± 25	

1. All the power (V_{DD} , V_{DDA}) And ground (V_{SS} , V_{SSA}) Pin must always be connected to the external power supply system within the allowed range.

2. $I_{INJ (PIN)}$ Must not exceed its limit, which is to ensure V_{IN} Do not exceed their maximum. If you can not guarantee V_{IN} Does not exceed its maximum value, but also to ensure that the outside limit system $I_{INJ (PIN)}$ Do not exceed their maximum. when $V_{IN} > V_{DD}$ When there is a positive injection current; when $V_{IN} < V_{SS}$ When there is a reverse injection current.

3. Reverse injection current will interfere with the analog performance of the device. See section 5.3.17 Section.

4. When several I / O While port injection current, $\Sigma I_{INJ (PIN)}$ The maximum value of the absolute values of the forward current is injected into the immediate injection current and the reverse. The results are based on Device 4 More I / O Ports on $\Sigma I_{INJ (PIN)}$ Maximum features.

table 5 Temperature characteristics

symbol	description	Numerical	unit
T_{STG}	Storage temperature	- 65 + 150	° C
T_J	The maximum junction temperature	150	° C

5.3 Working conditions

5.3.1. General working conditions

table 6 General working conditions

symbol	parameter	condition		Minimum	Maximum	Unit
f_{HCLK}	internal AHB Clock frequency			0	72	MHz
f_{PCLK1}	internal APB1 Clock frequency			0	36	MHz
f_{PCLK2}	internal APB2 Clock frequency			0	72	MHz
V_{DD}	Standard operating voltage			2	3.6	V
V_{DDA} (1)	The analog part of the operating voltage (not used ADC) Must V_{DD} (2) the same			2	3.6	V
	The analog part of the operating voltage (use ADC)			2.4	3.6	V
V_{BAT}	Backup section-operation voltage			1.8	3.6	V
V_{IN}	I / O Input voltage	standard I / O		-0.3	V_{DD}+ 0.3	
		FT I / O	2V <V_{DD} < 3.6V	-0.3	5.5	
			V_{DD} = 2V	-0.3	5.2	
		BOOT0		0	5.5	
P_D	Power Dissipation reference temperature 6 : T = 85 ° C Temperature label 7 : T = 105 ° C	LQFP100			434	mW
		LQFP64			444	mW
		LQFP48			363	mW
		QFN36			1000	mW
T_A	Ambient temperature (reference temperature 6)	Maximum power dissipation		- 40	85	° C
		Low power dissipation (4)		- 40	105	° C
	Ambient temperature (reference temperature 7)	Maximum power dissipation		- 40	105	° C
		Low power dissipation (4)		- 40	125	° C
T_J	Junction Temperature Range	Temperature label 6		- 40	105	° C
		Temperature label 7		- 40	125	° C

1. When ADC When, Table 43 .

2. It is recommended to use the same power supply as V_{DD} with V_{DDA} Power supply, and power during normal operation, V_{DD} with V_{DDA} Between allows up 300mV Difference.

3. in case T_A Low, as long as T_J No more than T_{Jmax} (See 1 Section), it allows higher P_D Value.

4. In the state of lower power dissipation, as long as T_J No more than T_{Jmax} (See 1 Section), T_A It can be extended to this range.

5.3.2. When the power-up and power-down working conditions

Parameters given in the table are the test results under normal operating conditions.

table 7 On power-up and power-down of Working conditions

symbol	parameter	condition	Minimum	Maximum	unit	
t_{VDD}	V_{DD} Rate rise		0	∞	μs / V	
	V_{DD} Rate of decline		20	∞		

5.3.3 Embedded reset and power control module characteristics

Parameters given in the table is based on the table 6 And at ambient temperature are listed in V_{DD} Test results under supply voltage.

table 8 Embedded reset and power control module Block properties

symbol	parameter	condition	Min	Typ	Max	Units	
V_{PVD}	Programmable voltage Selected level detector	PLS [2: 0] = 000 (Rising)	2.10	2.18	2.26	V	
		PLS [2: 0] = 000 (Falling edge)	2.00	2.07	2.16	V	
		PLS [2: 0] = 001 (Rising)	2.19	2.28	2.37	V	
		PLS [2: 0] = 001 (Falling edge)	2.09	2.17	2.27	V	
		PLS [2: 0] = 010 (Rising)	2.28	2.38	2.48	V	
		PLS [2: 0] = 010 (Falling edge)	2.18	2.27	2.38	V	
		PLS [2: 0] = 011 (Rising)	2.38	2.47	2.58	V	
		PLS [2: 0] = 011 (Falling edge)	2.28	2.37	2.48	V	
		PLS [2: 0] = 100 (Rising)	2.47	2.57	2.69	V	
		PLS [2: 0] = 100 (Falling edge)	2.37	2.46	2.59	V	
		PLS [2: 0] = 101 (Rising)	2.57	2.67	2.79	V	
		PLS [2: 0] = 101 (Falling edge)	2.47	2.56	2.69	V	
		PLS [2: 0] = 110 (Rising)	2.66	2.77	2.90	V	
		PLS [2: 0] = 110 (Falling edge)	2.56	2.66	2.80	V	
		PLS [2: 0] = 111 (Rising)	2.76	2.86	3.00	V	
		PLS [2: 0] = 111 (Falling edge)	2.66	2.76	2.90	V	
$V_{PVDhyst}$ (2)	PVD Sluggish			100			mV
$V_{POR / PDR}$	Power up / down complex	Falling	1.8 (1)	1.87	1.96	V	
	Bit Threshold	Rising	1.84	1.92	2.0	V	
$V_{PVDhyst}$ (2)	PDR Sluggish			40			mV
$T_{RSTTEMPO}$ (2)	Reset duration		1	2.5	4.5	ms	

1. Guaranteed by the design characteristics of the product to a minimum value $V_{POR / PDR}$.

2. Guaranteed by design, not tested in production.

5.3.4 Built-in reference voltage

Parameters given in the table is based on the table 6 And at ambient temperature are listed in V_{DD} Test results under supply voltage.

table 9 Built-in reference voltage

symbol	parameter	condition	Min	Typ	Max	Units	
V_{REFINT}	Built-in reference voltage	- 40 ° C <T_A < + 105 ° C	1.16	1.20	1.26	V	
		- 40 ° C <T_A < + 85 ° C	1.16	1.20	1.24	V	
$T_{S\_vrefint}$ (1)	When reading out the internal reference voltage, ADC Sampling time			5.1	17.1 (2)		μs

1. Guaranteed by the design characteristics of the product to a minimum value $V_{POR / PDR}$.

2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

Current consumption is a comprehensive index of various parameters and factors, these factors include parameters and operating voltage, ambient temperature, I / O Pin load, product software configuration, operating frequency, I / O The turnover rate of the foot, the position of the program codes and the like in the memory performed.

The method of measuring the current consumption of explanation, see FIG. 11 .

Current consumption in this section measured value in all operating modes given, are performed in a streamlined code can be obtained Dhrystone2.1 Code equivalent results.

Maximum current consumption

The microcontroller in the following conditions:

- all I / O Pins are in input mode, and is connected to a quiescent level on –V_{DD} or V_{SS} (No load).
- All the peripherals are turned off, unless otherwise stated.
- Flash memory access time to adjust f_{HCLK} Frequency of(0 ~ 24MHz When 0 A waiting period, 24 ~ 48MHz When 1 A waiting period, more than 48MHz When 2 Wait cycles).
- Instruction prefetch function is on (Note: This parameter must be set before setting the clock and bus division).
- When you turn on the peripherals: $f_{PCLK1} = f_{HCLK / 2}$, $f_{PCLK2} = f_{HCLK}$. table 10 ,table 11 And Table 12 The parameters given in the table is based 5 And at ambient temperature are listed in V_{DD} Test results under supply voltage.

table 10 Run mode Maximum current of the formula Eliminate Consumption, data Office Processing code runs from the internal flash memory

symbol parameter		condition	f_{HCLK}	The maximum (1)		unit
				T_A = 85 ° C	T_A = 105 ° C	
I_{DD}	Supply current in run mode	External clock (2) To enable all peripherals	72MHz	50	50.3	mA
			48MHz	36.1	36.2	
			36MHz	28.6	28.7	
			24MHz	19.9	20.1	
			16MHz	14.7	14.9	
			8MHz	8.6	8.9	
		External clock (2) Turn off all peripherals	72MHz	32.8	32.9	
			48MHz	24.4	24.5	
			36MHz	19.8	19.9	
			24MHz	13.9	14.2	
			16MHz	10.7	11	
			8MHz	6.8	7.1	

1. Derived from a comprehensive assessment, not tested in production.

2. External clock 8MHz , when f_{HCLK}> 8MHz When enabled PLL .

table 11 Run mode The maximum current consumption, the data Reason Code from the inside RAM Run

symbol parameter		condition	f_{HCLK}	The maximum (1)		unit
				T_A = 85 ° C	T_A = 105 ° C	
I_{DD}	Supply current in run mode	External clock (2) To enable all peripherals	72MHz	48	50	mA
			48MHz	31.5	32	
			36MHz	twenty four	25.5	
			24MHz	17.5	18	
			16MHz	12.5	13	
			8MHz	7.5	8	
		External clock (2) Turn off all peripherals	72MHz	29	29.5	
			48MHz	20.5	twenty one	
			36MHz	16	16.5	
			24MHz	11.5	12	
			16MHz	8.5	9	
			8MHz	5.5	6	

1. It derived from a comprehensive assessment to the production V_{DD} max with f_{HCLK} max Conditions for the test.

2. External clock 8MHz , when f_{HCLK}> 8MHz When enabled PLL .

table 12 Sleep Mode The maximum level under the formula flow Consumption, the code running Flash or RAM in

symbol parameter		condition	f_{HCLK}	The maximum (1)		unit
				T_A = 85 ° C T_A = 105 ° C		
I_{DD}	Supply current in sleep mode	External clock (2) To enable all peripherals	72MHz	30	32	mA
			48MHz	20	20.5	
			36MHz	15.5	16	
			24MHz	11.5	12	
			16MHz	8.5	9	
			8MHz	5.5	6	
		External clock (2) Turn off all peripherals	72MHz	7.5	8	
			48MHz	6	6.5	
			36MHz	5	5.5	
			24MHz	4.5	5	
			16MHz	4	4.5	
			8MHz	3	4	

1. It derived from a comprehensive assessment to the production V_{DD} max And to f_{HCLK} max Enabled peripherals for the conditions tested.

2. External clock 8MHz , when f_{HCLK}> 8MHz When enabled PLL .

table 13 Typical and maximum current consumption in the standby mode and shutdown

symbol parameter		condition	Typical values		Maximum		unit
			V_{DD} / V_{BAT} = 2.4V	V_{DD} / V_{BAT} = 3.3V	T_A = 85 ° C	T_A = 105 ° C	
I_{DD}	Supply current in shutdown mode	Regulator in run mode, low and high internal RC High-speed oscillator and the oscillator is turned off (no independent watchdog)	22.7	23.4 200		370	μA
		Regulator in low power mode, low and high internal RC High-speed oscillator and the oscillator is turned off (no independent watchdog)	9.1	10.3 180		340	
	The supply current in standby mode	Low-speed internal RC The oscillator is turned on and independent watchdog	2.4	2.06	-	-	
		Low-speed internal RC The oscillator is turned on, an independent watchdog is disabled	2.3	2.81	-	-	
		Low-speed internal RC Oscillator and independent watchdog in the closed state, low frequency oscillator RTC It is off	1.5	3.17	4	5	
I_{DD_VBAT}	Supply current backup area Low frequency oscillator RTC It is on		1.1	1.4	1.9 (2)	2.2	

1. Typical values are in T_A = 25 ° C Test available.

2. Derived from a comprehensive assessment, not tested in production.

Typical current consumption

MCU In the following conditions:

- all I / O Pins are in input mode, and is connected to a quiescent level on –V_{DD} or V_{SS} (No load).
- All the peripherals are turned off, unless otherwise stated.
- Flash memory access time to adjust f_{HCLK} Frequency of(0 ~ 24MHz When 0 A waiting period, 24 ~ 48MHz When 1 A waiting period, more than 48MHz When 2 Wait cycles).
- Ambient temperature and V_{DD} Supply voltages are listed in Table 6 .
- Instruction prefetch function is on (Note: This parameter must be set before setting the clock and bus division). When you turn on the peripherals:

  $f_{PCLK1} = f_{HCLK} / 4$, $f_{PCLK2} = f_{HCLK} / 2$, $f_{ADCCLK} = f_{PCLK2} / 4$.

table 14 Run mode Typical current consumption under the formula , From the internal data processing code Flash Run

symbol parameter		condition	f_{HCLK}	Typical values (1)		unit
				Enable all peripherals (2)	Turn off all peripherals	
I_{DD}	Supply current in run mode	External clock (3)	72MHz	32.46	21.7	mA
			48MHz	21.96	14.73	
			24MHz	12.13	8.57	
			8MHz	5.5	4.31	

1. Typical values are in T_A = 25 ° C , V_{DD} = 3.3V When the test result.

2. Each analog part ADC To add additional 0.8mA Current consumption. In the application environment, which in turn is only part of the current ADC (Set up ADC_CR2 Deposit The device ADON Will increase when the bit).

3. External clock 8MHz , when f_{HCLK}> 8MHz When enabled PLL .

table 15 Run mode Typical current consumption under the formula , Data processing code from the internal RAM Run

symbol parameter		condition	f_{HCLK}	Typical values (1)		unit
				Enable all peripherals (2)	Turn off all peripherals	
I_{DD}	Supply current in run mode	External clock (3)	72MHz	24.84	14.21	mA
			48MHz	17.17	10.05	
			24MHz	9.38	5.86	
			8MHz	4.07	2.92	

1. Typical values are in T_A = 25 ° C , V_{DD} = 3.3V When the test result.

2. Each analog part ADC To add additional 0.8mA Current consumption. In the application environment, which in turn is only part of the current ADC (Set up ADC_CR2 Deposit The device ADON Will increase when the bit).

3. External clock 8MHz , when f_{HCLK}> 8MHz When enabled PLL .

table 16 In sleep mode Typical electricity flow Consumption, the number of According to the internal processing code from Flash or RAM Run

symbol parameter		condition	f_{HCLK}	Typical values (1)		unit
				Enable all peripherals (2)	Turn off all peripherals	

I_{DD}	Supply current in sleep mode	External clock (3)	72MHz	17.57	17.61	mA

1. Typical values are in T_A = 25 ° C , V_{DD} = 3.3V When the test result.

2. Each analog part ADC To add additional 0.8mA Current consumption. In the application environment, which in turn is only part of the current ADC (Set up ADC_CR2 Deposit The device ADON Will increase when the bit).

3. External clock 8MHz , when f_{HCLK}> 8MHz When enabled PLL .

Built-in peripheral current consumption

Built-in peripheral current consumption is shown in Table 17 , MCU The working conditions are as follows:

- all I / O Pins are in input mode, and is connected to a quiescent level on –V_{DD} or V_{SS} (No load).
- All the peripherals are turned off, unless otherwise stated.
- The values given are derived by measuring the current consumption calculation
  - Turn off all peripheral clocks
  - Open only a peripheral clock
- Ambient temperature and V_{DD} Supply voltages are listed in Table 4 .

table 17 Inside Peripheral home Current consumption (1)

Built-in peripherals		25 ° C When the typical power consumption of the unit		Built-in peripherals	25 ° C Typical power when Consume	unit
APB1	TIM2	1.2	mA APB2	GPIOA	0.47	mA
	TIM3	1.2		GPIOB	0.47	
	TIM4	0.9		GPIOC	0.47	
	SPI2	0.2		GPIOD	0.47	
	USART2	0.35		GPIOE	0.47	
	USART3	0.35		ADC1 (2)	1.81	
	I_2C1	0.39		ADC2	1.78	
	I_2C2	0.39		TIM1	1.6	
	USB	0.65		SPI1	0.43	
	CAN	0.72		USART1	0.85	

1. f_{HCLK} = 72MHz , f_{APB1} = f_{HCLK} / 2 , f_{APB2} = f_{HCLK} , Pre-separation of each peripheral-frequency coefficient to the default value.

2. ADC Special conditions: f_{HCLK} = 56MHz , f_{APB1} = f_{HCLK} / 2 , f_{APB2} = f_{HCLK} , f_{ADCCLK} = f_{APB2} / 4 , ADC_CR2 Register ADON = 1 .

5.3.6 External clock source characteristics

Speed external clock from the external oscillation source user generated

Characteristic parameters given in the table is to use a high speed external clock source is measured, ambient temperature and supply voltage in accordance with Table 6 conditions of.

table 18 Speed external User clock unit characteristic

symbol	parameter	condition	Min	Typ	Max	Units		

f_{HSE_ext}	User external clock frequency (1)		1	8	25	MHz
V_{HSEH}	OSC_IN High voltage input pin		2.2		3.3 V	
V_{HSEL}	OSC_IN Low-level voltage input pin		0		2.2	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN High or low time (1)		5			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN Rise or fall time (1)				20	
$C_{in(HSE)}$	OSC_IN Input capacitance (1)			5		pF
DuCy (HSE)	Duty Cycle		45	50	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		0.3 ± 1		μA

1. Guaranteed by design, not tested in production.

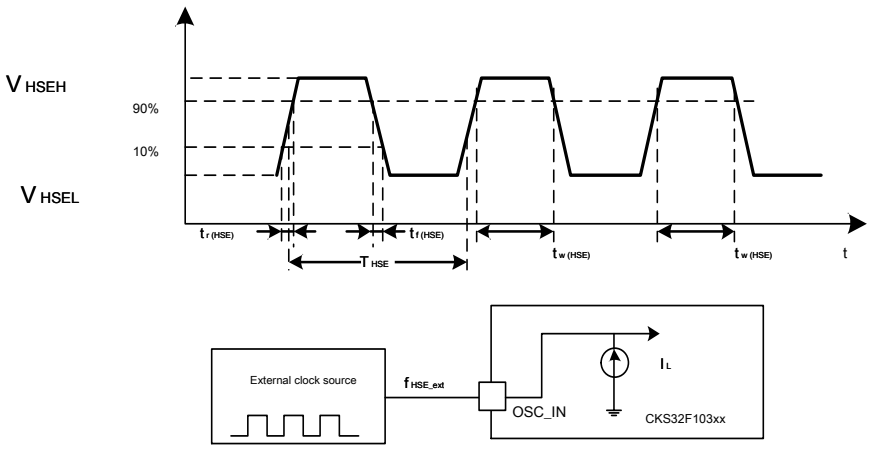
Low-speed external clock from the external oscillation source user generated

Characteristic parameters given in the table is to use a low-speed external clock source measured, ambient temperature and supply voltage in accordance with Table 6 conditions of.

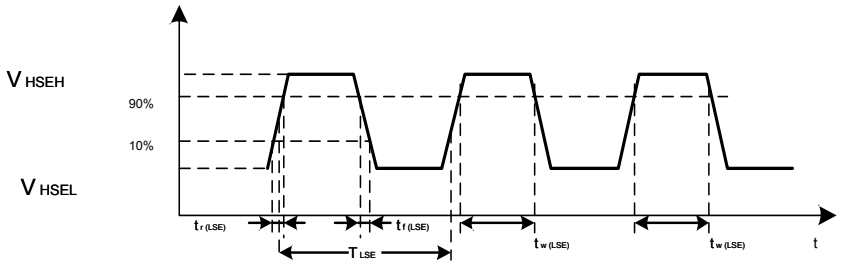
table 19 Low-speed external User clock characteristics

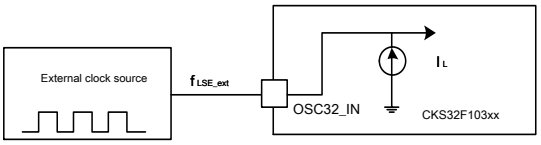
symbol	parameter	condition	Min	Typ	Max	Units
f_{LSE_ext}	User external clock frequency (1)		0	32.768	4000	KHz
V_{LSEH}	OSC32_IN High voltage input pin		1.8		3.3 V	
V_{LSEL}	OSC32_IN Low-level voltage input pin		0		1.7	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN High or low time (1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN Rise or fall time (1)				50	
$C_{in(LSE)}$	OSC32_IN Input capacitance (1)			5		pF
DuCy (LSE)	Duty Cycle		30	50	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		-0.4 ± 1		μA

1. Guaranteed by design, not tested in production.



Map 12 AC timing chart of the high-speed external clock source





Map 13 AC timing diagram of the external low speed clock source

High-speed external clock using a crystal / ceramic resonator generates

High-speed external clock (HSE) You can use a 4 ~ 16MHz Crystal oscillator / resonator configuration produces. The information given in this section are based on the use of the typical external components listed in the table, obtained by combining the characteristics evaluation results. In use, the resonator and the load capacitance of the oscillator must be as close as possible to the pin, in order to reduce the settling time and the start of output distortion.

table 20 HSE 4 ~ 16MHz Oscillator Characteristics (1) (2)

symbol	parameter	condition	Min	Typ	Max	unit
f_{OSC_IN}	Oscillator frequency		4	8	16	MHz
R_F	Feedback resistor			200		kΩ
C_{L1} C_{L2} (3)	Corresponding to the load capacitance and serial proposed crystal impedance (R_S) (4)	R_S = 30Ω		30		pF
i_2	HSE Drive current	V_{DD} = 3.3V , V_{IN} = V_{SS} 30pF load			1	mA
g_m	Transconductance oscillator	start up	25			mA / V
$t_{SU(HSE)}$ (5)	Start Time	V_{DD} stable		2		ms

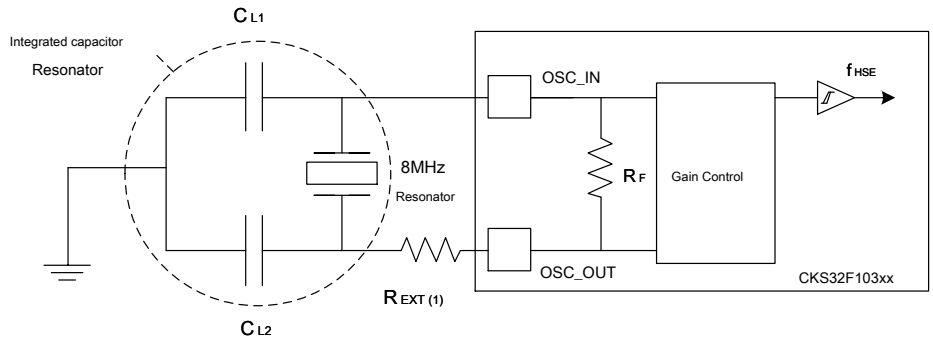
1. Characteristic parameter of the resonator is given by a crystal / ceramic resonator manufacturer.

2. Derived from a comprehensive assessment, not tested in production.

3. for C_{L1} with C_{L2} , Use quality, designed for high frequency applications (typical value) 5pF ~ 25pF Between the ceramic capacitor, and the selection of satisfactory crystalline Or resonator. usually C_{L1} with C_{L2} With the same parameters. Manufacturers typically crystalline C_{L1} with C_{L2} The serial combination of parameters given load capacitance. In selecting C_{L1} with C_{L2} Time, PCB with MCU Pin capacitance should be taken into account (it can be roughly the pin PCB By capacitive plate 10pF estimate).

4. Relatively low RF The resistance value, it is possible to provide protection to avoid problems when used in humid environments generated, leakage and bias conditions arising under this environment It has changed. However, when MCU Application in the harsh humid conditions, this parameter needs to be taken into account when designing.

5. $t_{SU(HSE)}$ Is a start-up time, is enabled from software HSE Begin until a stable 8MHz The oscillation period of time. This value is a standard crystal resonator The measured, it may be due to different manufacturers vary widely crystals.



Map 14 use 8MHz Typical applications of crystals

1. R_{EXT} Value determined by the characteristics of the crystal. Typical values are 5 to 6 Fold R_S .

Low-speed external clock using a crystal / ceramic resonator generates

Low-speed external clock (LSE) You can use a 32.768kHz Crystal oscillator / resonator configuration produces. The information given in this section are based on Table twenty one Typical external components listed in the evaluation of the results obtained by the integrated features. In use, the resonator and the load capacitance of the oscillator must be as close as possible to the pin, in order to reduce the settling time and the start of output distortion.

Note: For C_{L1} with C_{L2} We recommended to use high-quality 5pF ~ 15pF Between the ceramic capacitor, and meet the requirements of the selection or crystal resonator Device. usually C_{L1} with C_{L2} With the same parameters. Manufacturers typically crystalline C_{L1} with C_{L2} The serial combination of parameters given load capacitance. Load Capacitance C_L It is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$,among them C_{stray} It is the pin capacitance and PCB Board or PCB Capacitance associated, its typical value is between 2pF to 7pF between.

WARNING: To avoid exceeding C_{L1} with C_{L2} The maximum (15pF) Highly recommended load capacitance $C_L \leq 7$pF Resonator, the load can not be used Capacitance 12.5pF The resonator. For example: If one of the load capacitance $C_L = 6$pF Resonator and $C_{stray} = 2$pF ,then $C_{L1} = C_{L2} = 8$pF .

table 21 LSE Oscillator Characteristics ($f_{LSE} = 32.768$kHz) (1)

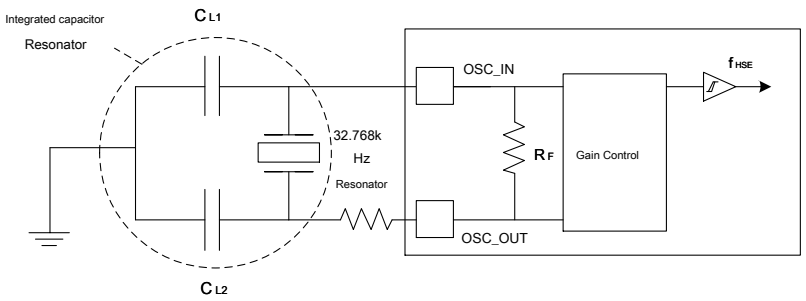
symbol	parameter	condition	Min	Typ	Max	Units
R_F	Feedback resistor			5		MΩ
C_{L1} C_{L2} (2)	Corresponding to the load capacitance and serial proposed crystal impedance (R_S) (3)	$R_S = 30k\Omega$			15	pF
I_2	LSE Drive current	$V_{DD} = 3.3V$, $V_{IN} = V_{SS}$			1.4 μA	
g_m	Transconductance oscillator		5			μA / V
$t_{SU(LSE)}$ (4)	Start Time	V_{DD} stable		3		s

1. Derived from a comprehensive assessment, not tested in production.

2. See cautions and warnings in this paragraph above the table.

3. With a smaller selection R_S Oscillator high value (e.g. MSIV-TIN32.768kHz) , Current consumption can be optimized.

4. $t_{SU(HSE)}$ Is a start-up time, is enabled from software HSE Measurement is started until a stable 8MHz The oscillation period of time. This value is a standard crystal Measured on a resonator, which may vary by manufacturer of crystals vary widely.



Map 15 use 32.768kH Typical applications of crystals

5.3.7 Characteristics of the internal clock source

Characteristic parameters given in the table is the use of ambient temperature and supply voltage in accordance with Table 6 Measured conditions.

High-speed internal (HSI) RC Oscillator

table 22 HSI Oscillator Characteristics (1) (2)

symbol	parameter	condition	Min	Typ	Max	Units
f_{HSI}	frequency			8		MHz
ACC_{HSI}	HSI Accuracy Oscillator	T_A = - 40 ~ 105 ° C	- 2		2.5%	
		T_A = - 10 ~ 85 ° C	-1.5		2.2%	
		T_A = 0 ~ 70 ° C	-1.3		2	%
		T_A = 25 ° C	-1.1		1.8%	
$t_{SU\ (HSI)}$	HSI Oscillator start-up time		1		2	μs
$I_{DD\ (HSI)}$	HSI Oscillator power			80	100	μA

1. V_{DD} = 3.3V , T_A = - 40 ~ 105 ° C Unless otherwise noted.

2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC Oscillator

table 23 LSI Vibration Special oscillator Of (1)

symbol	parameter	Min	Typ	Max	Units
$f_{LSI\ (2)}$	frequency	30	40	60	kHz
$t_{SU\ (LSI)\ (3)}$	LSI Oscillator start-up time			85	μs
$I_{DD\ (LSI)\ (3)}$	LSI Oscillator power		0.65	1.2 μA	

1. V_{DD} = 3.3V , T_A = - 40 ~ 105 ° C Unless otherwise noted.

2. Derived from a comprehensive assessment, not tested in production.

3. Guaranteed by design, not tested in production.

Low-power mode wakeup time

table twenty four Wake-up time is listed in a 8MHz of HSI RC Wake-up phase of the oscillator measured. Wake-up clock source used by the current operating mode may be:

- Down or standby mode: the clock source is RC Oscillator
- Sleep mode: the clock source is the clock all the time when entering a sleep mode using the ambient

temperature and power supply voltage in accordance with Table 6 Measured conditions.

table twenty four Low-power mode wakeup time

symbol	parameter	condition	Typical Unit	
$t_{WUSLEEP}$ (1)	Wake up from sleep mode	use HSI RC Wake-up Clock	1.7	
t_{WUSTOP} (1)	Wake-up from stop mode (regulator in run mode)	HSI RC Wake-up Clock = 2μs	2.6	μs
	Wake-up from stop mode (low power consumption mode regulator)	HSI RC Wake-up Clock = 2μs Regulator from the low power mode time = 5μs	5.1	
$t_{WUSTDBY}$ (3)	Wake-up from standby mode	HSI RC Wake-up Clock = 2μs Wake-up regulator from the closed mode time = 38μs	52	

1. Wake-up time is measured from the start of the event to wake the user program reads the first instruction.

5.3.8 PLL characteristic

table 25 Parameters listed is the supply voltage and the ambient temperature in accordance with Table 6 Measured conditions.

table 25PLL characteristic

symbol	parameter	Numerical			unit
		Min	Typ	Max	
f_{PLL_IN}	PLL The input clock (2)	1	8.0	25	MHz
	PLL The input clock duty ratio	40	50	60	%
f_{PLL_OUT}	PLL Frequency clock output	16		72	MHz
t_{LOCK}	PLL Lock time		43	200	μs

1. Derived from a comprehensive assessment, not tested in production.

2. Note that the correct multiplication factor, so that in accordance with PLL Such that the input clock frequency f_{PLL_OUT} It is within the allowable range.

5.3.9 Reservoir characteristics

Flash memory

Unless otherwise noted, all parameters are in T_A - - 40 ~ 105 ° C get.

table 26 Flash Memory Features

symbol	parameter	condition	Min	Typ	Max	Units
t_{prog}	16 Bit programming time	T_A = - 40 ~ 105 ° C	-	-	20	μs
t_{ERASE}	page(1K Bytes) erase time	T_A = - 40 ~ 105 ° C	-		2	ms
t_{ME}	Full chip erase	T_A = - 40 ~ 105 ° C	-		10	ms
I_{DD}	Supply Current	Read mode, f_{HCLK} = 72MHz , 2 A waiting period, VDD = 3.3V			21.6	mA
		Write / erase mode, f_{HCLK} = 72MHz , VDD = 3.3V			3	mA
		Standby mode, VDD = 3.3 ~ 3.6V			1	μA

1. Guaranteed by design, not tested in production.

table 27 Flash memory and the data lifespan Shelf Life limit

symbol	parameter	condition	Min	Typ	Max	Units
N_{END}	life	T_A = - 40 ~ 85 ° C (Suffix is 6) T_A = - 40 ~ 105 ° C (Suffix is 7)	100			Thousand
t_{RET}	Data retention	T_A = - 40-85 ° C Time	10			year

1. Derived from a comprehensive assessment, not tested in production.

5.3.10 EMC characteristic

Sensitivity test sample is tested in the comprehensive assessment of the product.

Feature EMS (Electromagnetic Susceptibility)

When running a simple application (by I / O Port Blink 2 More LED) , The test sample is applied 2 Kinds of electromagnetic interference until an error occurs, led Flashing indicates errors.

- **Electrostatic discharge (ESD) (** Positive discharge and negative discharge) is applied to the chip until a pin all functional errors. This test is in line with IEC 1000-4-2 standard.
- **FTB : in V_{DD} with V_{SS} Adopted a 100pF Applying a capacitor voltage transient burst (forward and reverse) until a functional error. This test is in line with IEC** 1000-4-4 standard. Chip reset system can resume normal operation. Test results are shown in the following table.

table 28 EMS characteristic

symbol	parameter	condition	Level / type
V_{FESD}	Applied to any I / O Feet, resulting in erroneous function of voltage limit.	V_{DD} = 3.3V , T_A = + 25 ° C , f_{HCLK} = 72MHz . meets the IEC 1000-4-2	2B
V_{EFTB}	in V_{DD} with V_{SS} On by 100pF Capacitance applied , Resulting in erroneous function of voltage transient burst limit	V_{DD} = 3.3V , T_A = + 25 ° C , f_{HCLK} = 72MHz . meets the IEC 1000-4-4	4A

Solid design software to avoid noise problems

In the device level EMC Evaluation and optimization is carried out in a typical application environment. It should be noted that good EMC Performance and user applications and specific software are closely related.

Therefore, it is recommended to implement the software EMC Optimization, and with EMC Related to certification testing.

Software recommendations

Process control software must include Runaway, such as:

- Corrupted program counter
- Unexpected reset
- The key data is corrupted (control registers .....)

Pre-certification test

Many common failure (unexpected reset and the program counter is damaged), it is possible by manually NRST The introduction of a low level or into a continuous on the crystal pins 1 The second low level to reproduce.

Making ESD Test, voltage can be applied directly beyond the requirements of the application on the chip, when the operation of detecting an unexpected place, part of the software needs to be enhanced to prevent the occurrence of an unrecoverable error.

Electromagnetic interference (EMI)

When you run a simple application (by I / O Port Blink 2 More LED) Monitoring chip emits electromagnetic fields. This Emissions test Compliance SAE J1752 / 3 Standard, which specifies the test load plate and pins.

table 29 EMI characteristic

symbol parameter		condition	Monitoring frequency band	The maximum (f_{HSE} / f_{HCLK})		unit
				8 / 48MHz	8 / 72MHz	
S_{EMI} Peak		V_{DD} = 3.3 V , T_A = 25 ° C , LQFP100 Package with IEC 61967-2	0.1 ~ 30MHz	12	12	dBμV
			30 ~ 130MHz	twenty two	19	
			130MHz ~ 1GHz	twenty three	29	
			SAM EMI level do not	4	4	-

5.3.11 Absolute maximum (electrical sensitivity)

Based on three different tests (ESD , LU) Using a specific measurement method, the chip strength test to determine the sensitivity of the performance of its electrical.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse and a second interval after a negative pulse) is applied to all pins in all the samples, the sample size and the number of pins associated power chip (3 sheet × (n + 1) Supply pins). This test is in line with JESD22-A114 / C101 standard.

table 30ESD Absolute Maximum Ratings

symbol	parameter	condition	Types of	The maximum (1)	unit
$V_{ESD\ (HBM)}$	Electrostatic discharge voltage (Human Body Model)	T = +25 ° C ,meets the JESD22-A114	2	2000	V
$V_{ESD\ (CDM)}$	Electrostatic discharge voltage (charging device model)	T = +25 ° C ,symbol Close JESD22-C101	II	500	

1. Derived from a comprehensive assessment, not tested in production.

Static latch

In order to evaluate the performance of the latch, you need 6 Carried out on samples 2 Complementary static latch-up testing:

- For each supply pin provides the supply voltage exceeds the limit.
- In each of the input, output and configurable I / O Injection current pin. This test is in

line with EIA / JESD 78A IC latch standards.

table 31 Electrical Sensitivity

symbol	parameter	condition	Types of
LU	Static latch class	T = +105 ° C ,meets the JESD78A II class A	

5.3.12 I / O Port characteristics

General purpose input / output characteristics

Unless otherwise specified, the following table lists the parameters in Table 6 Measured conditions. all I / O Ports are compatible CMOS with

TTL .

table 32 I / O Static characteristics

symbol	parameter	condition	Minimum	Typical values	Maximum	unit
V_{IL}	Low level input voltage	standard I / O Feet, input Low voltage	-	-	0.28 × (V_{DD}- 2V) + 0.8V	V
		FT I / O (1) Feet, input Low voltage			0.32 × (V_{DD}- 2V) + 0.75V	
		all I / O Mouth, in addition to BTOOT0			0.35 V_{DD}	
V_{IH}	High-level input voltage	standard I / O Pin, high voltage input	0.41 × (V_{DD}- 2V) + 1.3V			
		FT I / O foot(1) , A high level input voltage	0.42 × (V_{DD}- 2V) + 1V			
		all I / O Mouth, in addition to BTOOT0	0.65 V_{DD} (2)			

V_{hys}	standard I / O Foot Schmitt trigger voltage hysteresis (2)		200			mV
	5V tolerate I / O Foot Schmitt trigger voltage hysteresis (2)		5% V_{DD} (3)			
I_{lkg} Input leakage current (4)		$V_{SS} \le V_{IN} \le V_{DD}$ standard I / O port			± 1	μA
		V_{IN} = 5V , 5V Tolerance port			3	
R_{PU} Weak pull equivalent resistance (5)		$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD} Weak pull-down impedance (5)		$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I / O Pin capacitance			5		pF

1. FT = 5V tolerate.

2. Schmitt trigger switching hysteresis voltage level. Derived from a comprehensive assessment, not tested in production.

3. Voltage is at least 100mV .

4. If the pin intrusion reverse current, leakage current may be higher than a maximum value adjacent.

5. Pullup and pulldown resistor is designed as a real resistor in series with a switchable PMOS / NMOS achieve. This one PMON / NMOS Switch resistance is very small (about Take up 10%) .

all I / O Ports are CMOS with TTL Compatible (without software configuration), their characteristics considered most stringent CMOS Process or TTL parameter:

- for V_{IH} :
  - in case V_{DD} Between [2.00V ~ 3.08V] ;use CMOS But contains characteristics TTL .
  - in case V_{DD} Between [3.08V ~ 3.60V] ;use TTL But contains characteristics CMOS .
- for V_{IL} :
  - in case V_{DD} Between [2.00V ~ 2.28V] ;use TTL But contains characteristics CMOS .
  - in case V_{DD} Between [2.28V ~ 3.60V] ;use CMOS But contains characteristics TTL .

Output drive current

GPIO (General purpose input / output port) or an output can absorb up to +/- 8mA Current and absorbs + 20mA Current (not strictly V) . In the user application, I / O The number of feet must ensure that the drive current can not exceed 5.2 Absolute Maximum Ratings section given below:

- all I / O From Port V The sum of the currents acquired, plus MCU in V On obtaining maximum operating current can not exceed the absolute maximum ratings IVDD (Table 4) .
- all I / O And from the port absorption V The sum of the currents flowing, plus MCU in V The maximum operating current flowing on, can not exceed the absolute maximum ratings IVSS (Table 4) .

The output voltage

Unless otherwise specified, the table 33 Parameters listed are ambient temperature and V_{DD} Supply voltage in accordance with Table 6 Measured conditions. all I / O Ports are compatible CMOS with TTL of.

table 33 Output voltage characteristic

symbol	parameter	condition	Minimum Maximum Unit		
$V_{OL\ (1)}$	Output low, when 8 Pins while absorbing current CMOS port, I_{IO} +			0.4	
$V_{OH\ (2)}$	Output high, when 8 While the output current pin	+ 8mA 2.7V <V_{DD} < 3.6V	V_{DD}- 0.4		
$V_{OL\ (1)}$	Output low, when 8 Pins while absorbing current TLL port, I_{IO} = + 8mA			0.4	
$V_{OH\ (2)\ (3)}$	Output high, when 8 While the output current pin	2.7V <V_{DD} < 3.6V	2.4		V
$V_{OL\ (1)\ (3)}$	Output low, when 8 Pins while absorbing current	I_{IO} = + 20mA		1.3	
$V_{OH\ (2)\ (3)}$	Output high, when 8 While the output current pin	2.7V <V_{DD} < 3.6V	2.4		
$V_{OL\ (1)\ (3)}$	Output low, when 8 Pins while absorbing current	I_{IO} = + 6mA		0.4	
$V_{OH\ (2)\ (3)}$	Output high, when 8 While the output current pin	2V <V_{DD} < 2.7V	V_{DD}- 0.4		

1. Absorption of current chip I_{IO} We must always follow the table 4 Given the absolute maximum ratings at the same time I_{IO} The sum of (all I / O Foot and control pins) must not exceed I_{VSS} .

2. Chip output current I_{IO} We must always follow the table 4 Given the absolute maximum ratings at the same time I_{IO} The sum of (all I / O Foot and control pins) must not exceed I_{VDD} .

3. Derived from a comprehensive assessment, not tested in production.

AC input and output characteristics

AC input-output characteristics of the definition and values respectively in FIG. 16 And Table 34 Given. Unless otherwise indicated, the listed parameters is the supply voltage and the ambient temperature in accordance with Table 6 Measured conditions.

table 34 AC input-output characteristics (1)

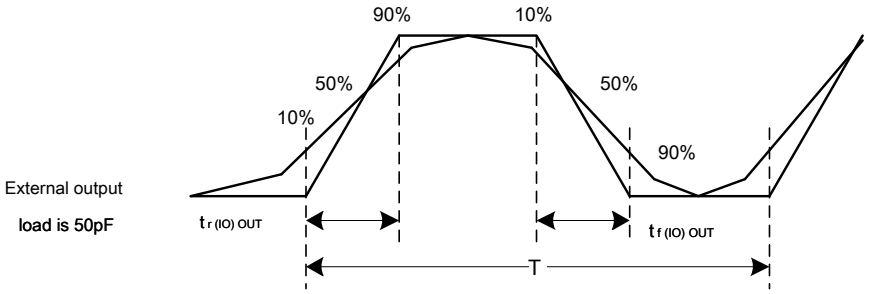
MODEx [1: 0] symbol		parameter	condition	Minimum Maximum Unit		
10 (2MHz)	$f_{max\ (IO)\ out}$	The maximum frequency (2)	C_L = 50 pF, V_{DD} = 2 ~ 3.6V		2	MHz
	$t_{f\ (IO)\ out}$	High output fall time to low	C_L = 50 pF, V_{DD} = 2 ~ 3.6V		125 (3)	ns
	$t_{r\ (IO)\ out}$	Up to a high level output rise time			125 (3)	
01 (10MHz)	$f_{max\ (IO)\ out}$	The maximum frequency (2)	C_L = 50 pF, V_{DD} = 2 ~ 3.6V		10 MHz	
	$t_{f\ (IO)\ out}$	High output fall time to low	C_L = 50 pF, V_{DD} = 2 ~ 3.6V		25 (3)	ns
	$t_{r\ (IO)\ out}$	Up to a high level output rise time			25 (3)	
11 (50MHz)	$f_{max\ (IO)\ out}$	The maximum frequency (2)	C_L = 30 pF, V_{DD} = 2.7 ~ 3.6V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 ~ 3.6V		30	
			C_L = 50 pF, V_{DD} = 2 ~ 2.7V		20	
	$t_{f\ (IO)\ out}$	High output fall time to low	C_L = 30 pF, V_{DD} = 2.7 ~ 3.6V		5 (3)	ns
			C_L = 50 pF, V_{DD} = 2.7 ~ 3.6V		8(3)	
			C_L = 50 pF, V_{DD} = 2 ~ 2.7V		12 (3)	
	$t_{r\ (IO)\ out}$	Up to a high level output rise time	C_L = 30 pF, V_{DD} = 2.7 ~ 3.6V		5 (3)	
			C_L = 50 pF, V_{DD} = 2.7 ~ 3.6V		8(3)	

			C_L = 50 pF, V_{DD} = 2 ~ 2.7V		12 (3)	
-	t_{EXTIpw}	EXTI The controller detects the external signal No pulse width		10		ns

1. I / O Port speed by MODEx [1: 0] Configuration. See also CKS32F103x8 with CKS32F103xB Reference manual on GPIO Port Configuration Register instruction of.

2. The maximum frequency chart 16 Defined.

3. Guaranteed by design, not tested in production.



in case ($t_r + t_f$) ≤ 2 / 3T And the duty cycle (45-55%) When the load is 50pF

When the maximum frequency

Map 16 AC input-output characteristic is defined

5.3.13 NRST Pin Characteristics

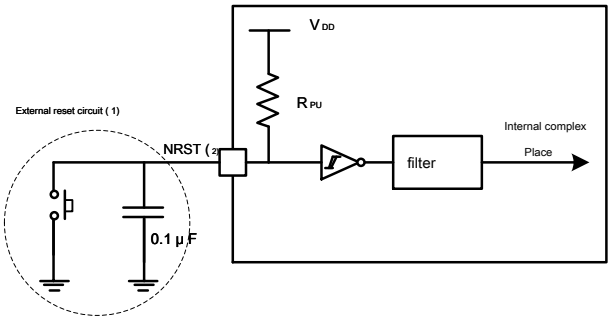
NRST Pin drivers to use CMOS Process, it can not disconnect the connection of a pull-up resistor, R_{PU} (Table 32) . Unless otherwise specified, the table 35 Parameters listed are ambient temperature and V_{DD} Supply voltage in accordance with Table 6 Measured conditions.

table 35NRST Special pins Sex

symbol	parameter	condition	Min	Typ	Max	Units
$V_{IL (NRST) (1)}$	NRST Input low voltage		-0.5		0.8	V
$V_{IH (NRST) (1)}$	NRST Input High Voltage		2		V_{DD} + 0.5	
$V_{hys (NRST) (1)}$	NRST Schmitt trigger voltage late Stagnant			200		mV
R_{PU}	Weak pull equivalent resistance (2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F (NRST) (1)}$	NRST Filtering the input pulse				100	ns
$V_{NF (NRST) (1)}$	NRST Non-filtered input pulse		300			ns

1. Guaranteed by design, not tested in production.

2. Pull-up resistor is designed as a real resistor in series with a switchable PMOS achieve. This one PMON / NMOS Switch resistance is very small (approximately 10%) .



Map 17 suggested NRST Pin protection

1. Network is reset to prevent parasitic reset.

2. The user must ensure that NRST Table can be lower than the potential of the pin 35 The largest listed $V_{IL(NRST)}$ Or less, or MCU It can not be reset.

5.3.14 TIM Features of Timer

table 36 The parameters listed guaranteed by design.

For multiplexed input and output (output compare function pin, input capture, external clock, PWM Output) features details on participation 5.3.12 Section.

table 36TIMx (1) characteristic

symbol	parameter	condition	Minimum	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
f_{EXT}	CH1 to CH4 Timer external clock frequency		0	$f_{TIMxCLK}$ / 2	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
Res_{TIM}	Timer Resolution			16	bit
$t_{COUNTER}$	When the selected internal clock, 16 Bit counter clock cycle		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz 0.0139		910	µs
t_{MAX_COUNT}	The maximum possible count			65536x65536 $t_{TIMxCLK}$	
		$f_{TIMxCLK}$ = 72MHz		59.6	s

1. TIMx Is a generic name, on behalf of TIM1 ~ TIM4 .

5.3.15 Communication Interface

I2 C Interface Features

Unless otherwise specified, the table 50 table 37 Parameter list is the use of ambient temperature, f_{PCLK1} Frequency and V Supply voltage in accordance with Table 6 Measured conditions.

CKS32F103x8 with CKS32F103xB Standard product I2 C Interface standard I2 C Communication protocol, but with the following limitations: SDA with SCL No " true " Open drain pin, when configured as an open drain output, and the pin-out V_{DD} between PMOS Tube is closed, but still exists.

I2 C Interface characteristics are listed in Table 37 Relevant input and output multiplexing function pin (SDA with SCL) The characteristic details, see page 5.3.12 Section.

table 37I2 C Interface Features

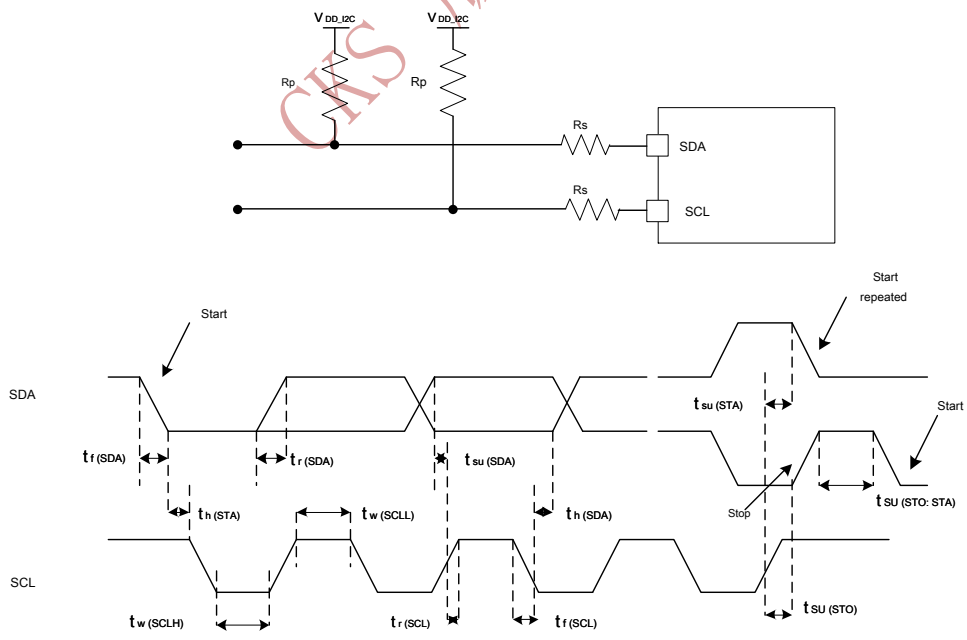
symbol	parameter	standard I2C (1)		fast I2C (1) (2)		unit
		maximum value	minimum value	Maximum	Minimum	
$t_{w(SCLL)}$	SCL Clock Time Low	4.7		1.3		μs
$t_{wSCLH)}$	SCL High Time Clock	4.0		0.6		
$t_{su(SDA)}$	SDA Settling Time	250		100		ns
$t_{h(SDA)}$	SDA Data Hold Time	0 (3)		0 (4)	900 (3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA with SCL Rise Time		1000	20 + 0.1C_b	300	
$t_{fSDA)}$ $t_{fSCL)}$	SDA with SCL Fall Time		300		300	
$t_{h(STA)}$ Start Condition Hold Time		4.0		0.6		μs
$t_{su(STA)}$ Repeat start condition setup time		4.7		0.6		
$t_{su(STO)}$ Stop Condition Setup Time		4.0		0.6		μs
$t_{w(STO:STA)}$	Stop condition to condition the start time (bus idle)	4.7		1.3		μs
C_b	Each bus capacitive load		400		400	pF

1. Guaranteed by design, not tested in production.

2. To achieve the standard mode I2C The maximum frequency, f_{PCLK1} It must be greater than 2MHz . In order to achieve fast mode I2C The maximum frequency, f_{PCLK1} It must be greater than 4MHz .

3. If you are not required to stretch SCL Low time signal, just beginning to meet the conditions of maximum hold time.

4. To leap SCL Falling undefined area, MCU Must ensure that internal SDA The signal of at least 300ns Hold time.



Map 18 I2C Bus and AC waveform measuring circuit (1)

1. Measurement points provided in CMOS Level: 0.3V_{DD} with 0.7V_{DD} .

table 38SCL frequency(f_{PCLK1} = 36MHz , V_{DD} = 3.3V) (1) (2)

f_{SCL} (kHz)	I2C_CCR Numerical

	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = An external pullup resistor, f_{SCL} = I2C speed.

2. for 200kHz About speed, speed error is ± 5% . For other speed range, the speed error is ± 2% . These external changes depending on design ELEMENTS

Precision parts.

SPI Interface Features

Unless otherwise specified, the table 39 Parameter list is the use of ambient temperature, f_{PCLKx} Frequency and V_{DD} Supply voltage in accordance with Table 6 Measured conditions.

About the input and output alternate-function pin (NSS , SCK , MOSI , MISO) The characteristic details, see page 5.3.12 Section.

table 39SPI characteristic(1)

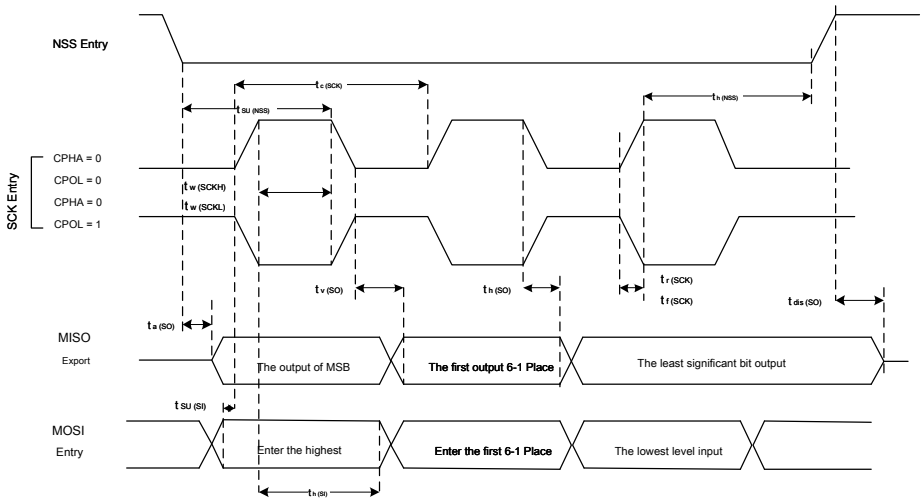
symbol	parameter	condition	Minimum	Maximum	Unit
f_{SCK} $1 / t_{c(SCK)}$	SPI Clock frequency	Main Mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI Clock rise and fall times	Load Capacitance: C = 30pF	- 8		ns
Ducy (SCK)	Slave clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (2)	NSS Settling Time	Slave mode	$4t_{PCLCK}$	-	ns
$t_{h(NSS)}$ (2)	NSS Hold Time	Slave mode	$2t_{PCLCK}$	-	
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK High and low time	Main mode, f_{PCLK} = 36MHz , Prescale = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time, the main mode	Main Mode	5		
$t_{su(SI)}$ (2)		Slave mode	5		
$t_{h(MI)}$ (2)	Data input hold time, the main mode	Main Mode	5		
$t_{h(SI)}$ (2)		Slave mode	4		
$t_{a(SO)}$ (2) (3)	Output data access time	From the model, f_{PCLK} = 20MHz	0	$3t_{PCLCK}$	
$t_{dis(SO)}$ (2) (4)	Data Output disable time	Slave mode	2	10	
$t_{v(SO)}$ (2) (1)	Output data valid time	From mode (enabled after the edge)		25	
$t_{v(MO)}$ (2) (1)	Output data valid time	Main Mode (enabled after the edge)		5	
$t_{h(SO)}$ (2)	Data output hold time	From mode (enabled after the edge)	15		
$t_{h(MO)}$ (2)		Main Mode (enabled after the edge)	2		

1. Remapping SPI1 Properties need to be further determined.

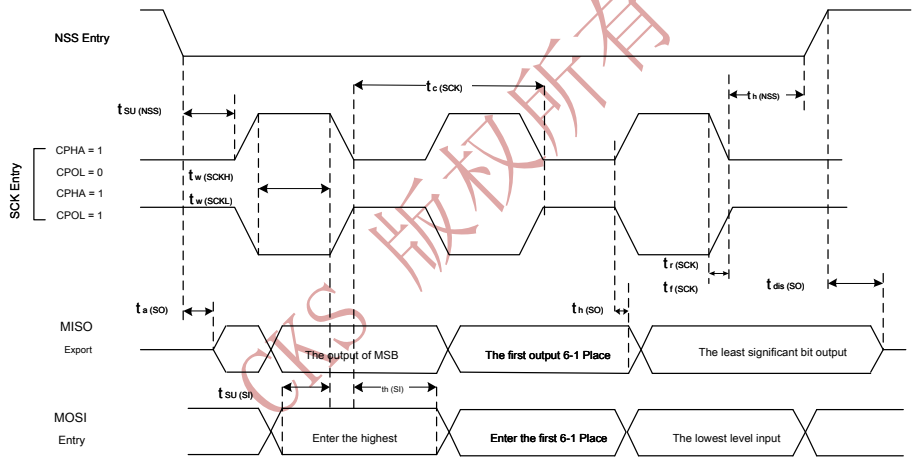
2. Derived from a comprehensive assessment, not tested in production.

3. Represents the minimum value of the minimum time to drive the output, the maximum value obtained represents the maximum time the correct data.

4. Represents the minimum value of the output of the minimum off time, maximum data line represents the maximum time a high-impedance state.

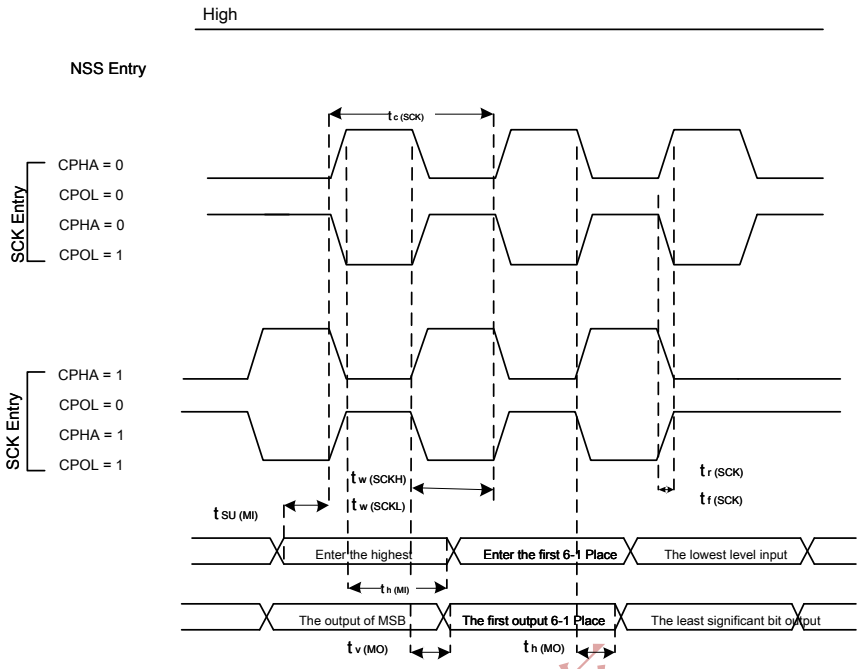


Map 19SPI FIG Timing - Slave mode and CPHA = 0



Map 20SPI Timing diagram - From the patterns and CPHA = 1 (1)

1 . Measurement points provided in CMOS Level: 0.3V DD with 0.7V DD .



Map 21SPI Timing Diagram - Master Mode (1)

1 . Measurement points provided in CMOS Level: 0.3V_{DD} with 0.7V_{DD} .

USB characteristic

USB(Full Speed) interface is through USB-IF Certification.

table 40USB Start Time

symbol	parameter	Maximum	unit
$t_{STARTUP}$ (1)	USB Transceiver start time	1	μs

1. Guaranteed by design, not tested in production.

table 41USB DC Characteristics

symbol	parameter	condition	Minimum (1)	The maximum (1)	unit
Input Level					
V_{DD}	USB Operating voltage (2)		3.0 (3)	3.6	V
V_{DI} (4)	Differential input sensitivity	I (USBDP, USBDM)	0.2		V
V_{CM} (4)	Differential common mode range	contain V_{DI} range	0.8	2.5	
V_{SE} (4)	Single-ended receiver threshold		1.3	2.0	
Output level					
V_{OL}	Static output low 1.5kΩ of R_L Connected to 3.6V (5)			0.3	V
V_{OH}	Static output high 15kΩ of R_L Connected to V_{SS} (5)		2.8	3.6	

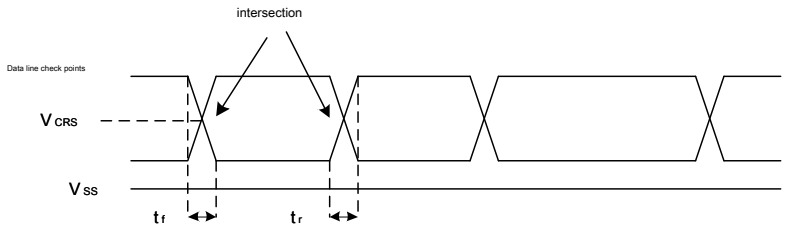
1. All measurements are subject to a voltage ground terminal device.

2. In order to USB 2.0 Full-speed electrical specifications compatible, USBDP (D +) It must pass a pin 1.5kΩ Resistor to 3.0 ~ 3.6V Voltage.

3. CKS32F0103xx correct USB Function can 2.7V Guaranteed, but not in 2.7 ~ 3.0V Range voltage level drops electrical characteristics.

4. A comprehensive assessment to ensure, not tested in production.

5. R_L It is connected to USB The load on the drive.



Map 22USB Timing: data signal rise and fall time is defined

table 42USB Full-speed electrical characteristics (1)

symbol	parameter	condition	Minimum	Maximum	unit
t_r	Rise Time(2)	CL ≤ 50pF	4	20	ns
t_f	Fall Time (2)	CL ≤ 50pF	4	20	ns
t_{rfm}	Rise and fall time matching	t_r / t_f	90	110	%
V_{CRS}	CROSS voltage output signal		1.3	2.0	V

1. Guaranteed by design, not tested in production.

2. Signal from the measurement data 10% to 90% .

5.3.16 CAN (Controller Area Network) interface

About the input and output alternate-function pin (CAN_TX with CAN_RX) The characteristic details, see page 5.3.12 Section.

5.3.17 12 Place ADC characteristic

Unless otherwise specified, the table 43 The argument is consistent with the use of table 6 Ambient temperature conditions, f_{PCLK2} Frequency and V_{DDA} Supply voltage measured.

Note: It is recommended to perform a calibration at each power-up.

table 43ADC characteristic

symbol	parameter	condition	Minimum	Typical	Max	Unit
V_{DDA}	Supply voltage	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	in V Input voltage feet	-	-	160 (1)	220 (1)	μA
f_{ADC}	ADC Clock frequency	-	0.6	-	14	MHz
f_S (2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14MHz	-	-	823	kHz
		-	-	-	17	1 / f_{ADC}

V_{AIN} (3)	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} Connected to ground)	- V_{REF+}		V
R_{AIN} (2)	External input impedance		-	-	50	kΩ
R_{ADC} (2)	Sampling switch resistance		-	-	1	kΩ
C_{ADC} (2)	Internal sample and hold capacitor				8	pF
t_{CAL} (2)	Calibration time	f_{ADC} = 14MHz	5.9			μs
			83			1 / f_{ADC}
t_{lat} (2)	Injection trigger a transition delay	f_{ADC} = 14MHz			0.214	μs
					3 (4)	1 / f_{ADC}
t_{latr} (2)	Conventional conversion trigger delay	f_{ADC} = 14MHz			0.143	μs
					2(4)	1 / f_{ADC}
t_S (2)	sampling time	f_{ADC} = 14MHz	0.107		17.1	μs
			1.5		239.5	1 / f_{ADC}
t_{STAB} (2)	Power-on time		0	0	1	μs
t_{CONV} (2)	The total conversion time	f_{ADC} = 14MHz	1		18	μs
	(Including sampling time)		14 to 252 (sampling t_S + Successive approximation 12.5)			1 / f_{ADC}

1. A comprehensive assessment to ensure, not tested in production.

2. Guaranteed by design, not tested in production.

3. in QFN36 , LQFP48 with LQFP64 Packaging products, V_{REF+} Internally connected to V_{DDA} , V_{REF-} Internally connected to V_{SSA} . See Table 2 .

4. For external trigger, you must watch 43 Delay listed plus a delay 1 / f_{PCLK2} .

formula 1 :maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2}) - R_{ADC}}$$

The above equation (Equation 1) For determining the maximum external impedance, such that the error may be less than 1/4 LSB . among them N = 12 (Show 12 Bit resolution).

table 44 f_{ADC} = 14MHz (1) The maximum R_{AIN}

T_S (cycle)	t_S (μs)	maximum R_{AIN} (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.1	-

1. Guaranteed by design, not tested in production.

table 45ADC Accuracy - Limitations of the test conditions (1) (2)

symbol	parameter	Test Conditions	Typical values	The maximum (3)	unit
ET	Comprehensive error	f_{PCLK2} = 56 MHz f_{ADC} = 14 MHz , R_{AIN} < 10 kΩ , V_{DDA} = 3 ~ 3.6V , T_A = 25 ° C Measurements were ADC After the calibration performed	± 1.3	± 2	LSB
EO	Offset error		± 1	± 1.5	
EG	Gain Error		± 0.5	± 1.5	
ED	Differential linearity error		± 0.7	± 1	
EL	Integral linearity error		± 0.8	± 1.5	

1. ADC DC precision value is measured after internal calibration.

2. ADC Accuracy of the relationship between the injection current and the reverse: the need to avoid reverse current is injected on any standard analog input pin, as this significantly reduced, further Analog input pin on an ongoing conversion accuracy. Recommendations on the pins may produce a standard analog reverse injection current (between pin and ground) increases a SCHOTT Group diode.

   If positive injection current, as long as in the first 5.3.12 Given in Section $I_{INJ(PIN)}$ with $\Sigma I_{INJ(PIN)}$ Within range, it will not affect ADC Accuracy.

3. A comprehensive assessment to ensure, not tested in production.

table 46ADC Accuracy (1) (2) (3)

symbol	parameter	Test Conditions	Typical values	The maximum (3)	unit
ET	Comprehensive error	f_{PCLK2} = 56 MHz f_{ADC} = 14 MHz , R_{AIN} < 10 kΩ , V_{DDA} = 2.4 ~ 3.6V Measurements were ADC After the calibration performed	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain Error		± 1.5	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

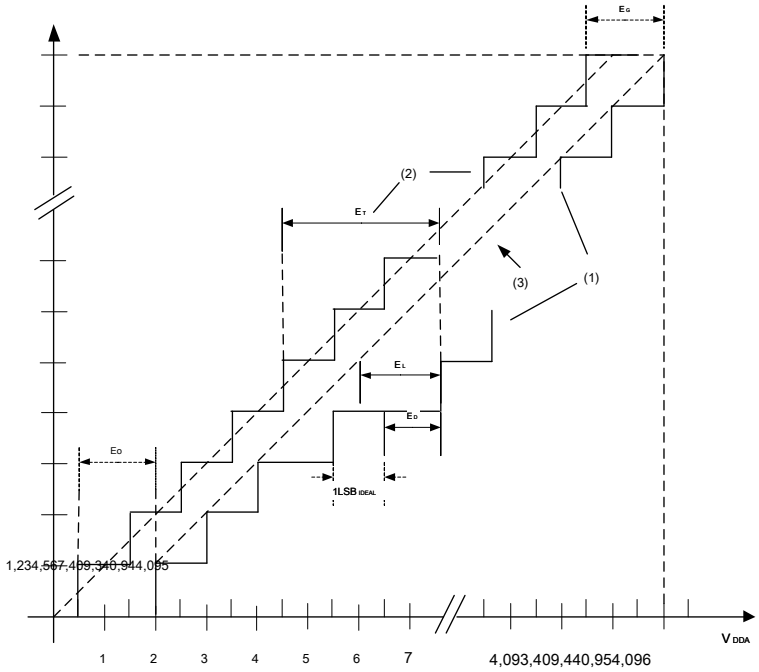
1. ADC DC precision value is measured after internal calibration.

2. Optimal performance can be limited V_{DD} ,frequency, V_{REF} And at a temperature range achieved.

3. ADC Accuracy of the relationship between the injection current and the reverse: the need to avoid reverse current is injected on any standard analog input pin, as this significantly reduced, further Analog input pin on an ongoing conversion accuracy. Recommendations on the pins may produce a standard analog reverse injection current (between pin and ground) increases a SCHOTT Group diode.

   If positive injection current, as long as in the first 5.3.12 Given in Section $I_{INJ(PIN)}$ with $\Sigma I_{INJ(PIN)}$ Within range, it will not affect ADC Accuracy.

4. A comprehensive assessment to ensure, not tested in production.



Map 23ADC Accuracy characteristics

(1) The actual ADC Examples of the conversion curve

(2) Ideal curve

(3) The actual transition point connection

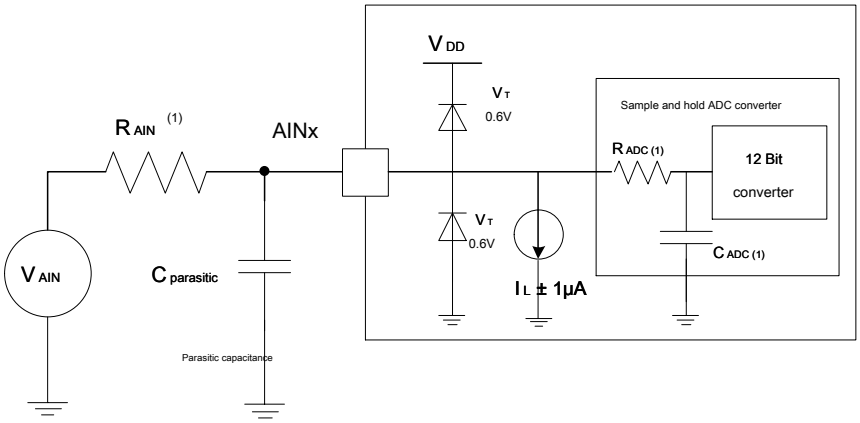
E_T Integrated error: the actual curve with a maximum deviation between the ideal transfer curve.

Eo Offset error: the first transition of the actual curve and the ideal curve of the transition time difference.

E_G Gain error: the last transition and the last transition of the difference between the ideal transfer curve in the actual transfer curve.

E_D Differential linearity error: the actual curve over ho ho from the distance (1LSB) Difference. among them $1LSB_{IDEAL} = V_{REF+} / 4096$ (or $V_{DDA} / 4096$, Determined by the package).

E_L Integral linearity error: maximum deviation between the actual conversion curve and the end connection.



Map twenty four use ADC FIG typical connection

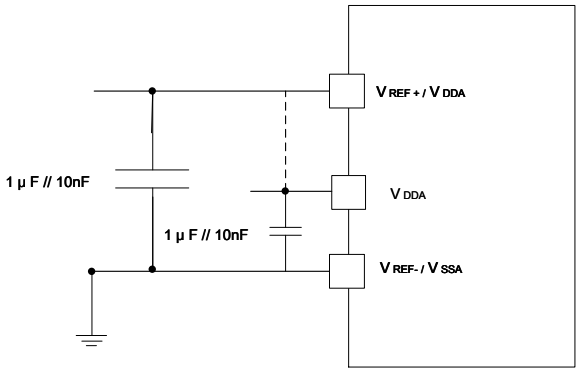
1. related R_{AIN} , R_{ADC} with C_{ADC} Values, see Table 46 .

2. Cparasitic Show PCB (Welding and PCB Quality-related layout) the parasitic capacitance at the pad (about 7pF) . larger Cparasitic It will reduce the value of the fine converter

Degree, the solution is to reduce the f_{ADC} .

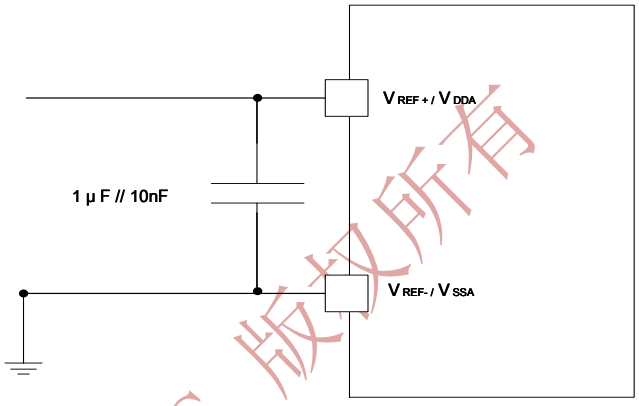
PCB Design Recommendations

in accordance with V_{REF+} Whether V_{DDA} Is connected, the power supply must be decoupled in Figure 25 Or diagram 26 connection. Figure 10nF Ceramic capacitor capacitance must be, they should be as close as possible MCU chip.



Map 25 Power supply and the reference power supply decoupling circuit (V_{REF+} Not with V_{DDA} Connected)

1. V_{REF+} with V_{REF-} Enter only appear in 100 Feet above product.



Map 26 Power supply and the reference power supply decoupling circuit (V_{REF+} versus V_{DDA} Connected)

1. V_{REF+} with V_{REF-} Enter only appear in 100 Feet above product.

5.3.18 Temperature sensor characteristics

table 47 Temperature sensor characteristics

symbol	parameter	Min	Typ	Max	Units
T_{L} (1)	V_{SENSE} Linearity with respect to temperature		± 1	± 2	° C
Avg_Slope (1)	Average slope	4.0	4.3	4.6	mV / °C
V_{25} (1)	in 25ºC When the voltage	1.61	1.62	1.63	V
t_{START} (2)	Settling Time	4		10	µs
T_{S_temp} (2) (3)	When reading the temperature, ADC sampling time			17.1	µs

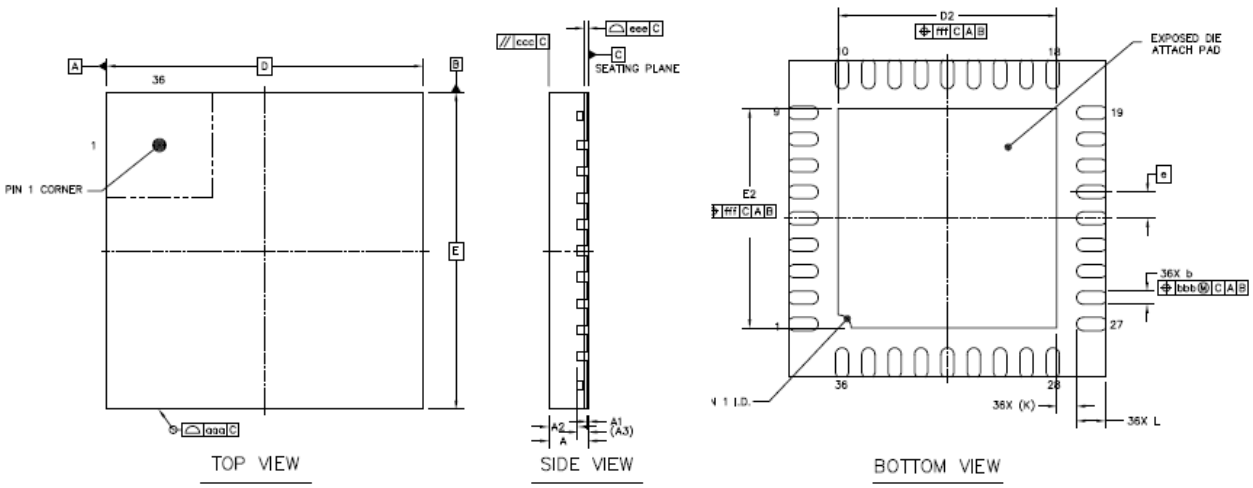
1. A comprehensive assessment to ensure, not tested in production.

2. Guaranteed by design, not tested in production.

3. The shortest sampling time can be recycled many times determined by the application through.

6. Package Characteristics

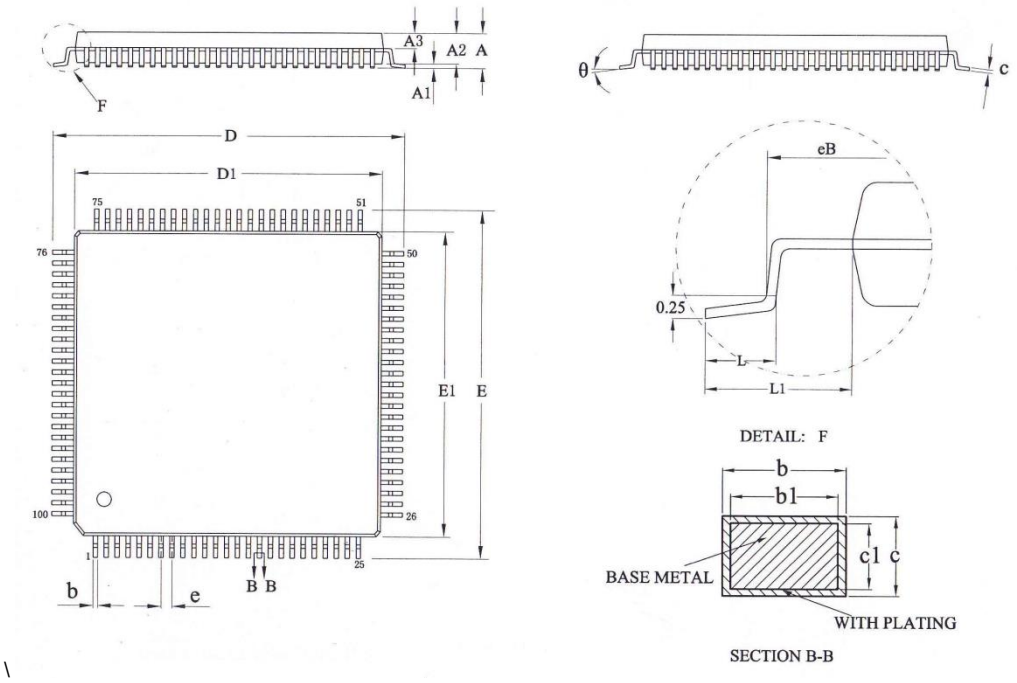
6.1 Package mechanical data



Map 27QFN36 Package FIG.

table 48QFN36 Package mechanical data

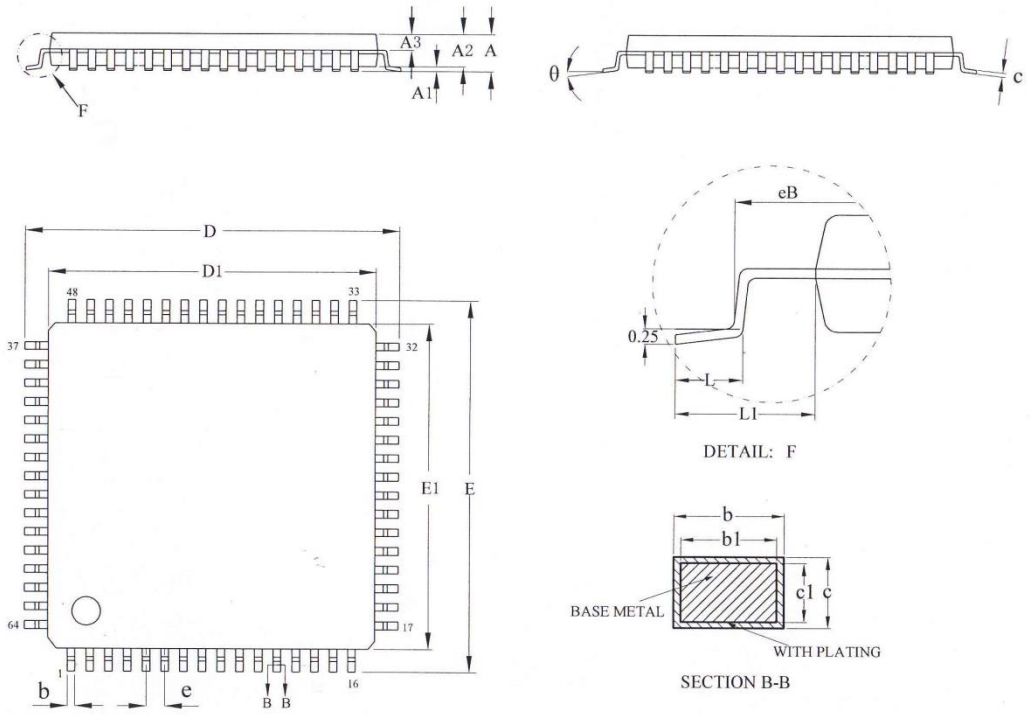
Grade	Millimeter		
	Minimum	Typical values	Maximum
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	6 BSC		
E	6 BSC		
e	0.5 BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
K	0.375 REF		
L	0.45	0.55	0.65
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		



Map 28LQFP100 , 100 Pin low profile quad flat package of FIG.

table 49LQFP100 , 100 Low square cross section pin flat package data

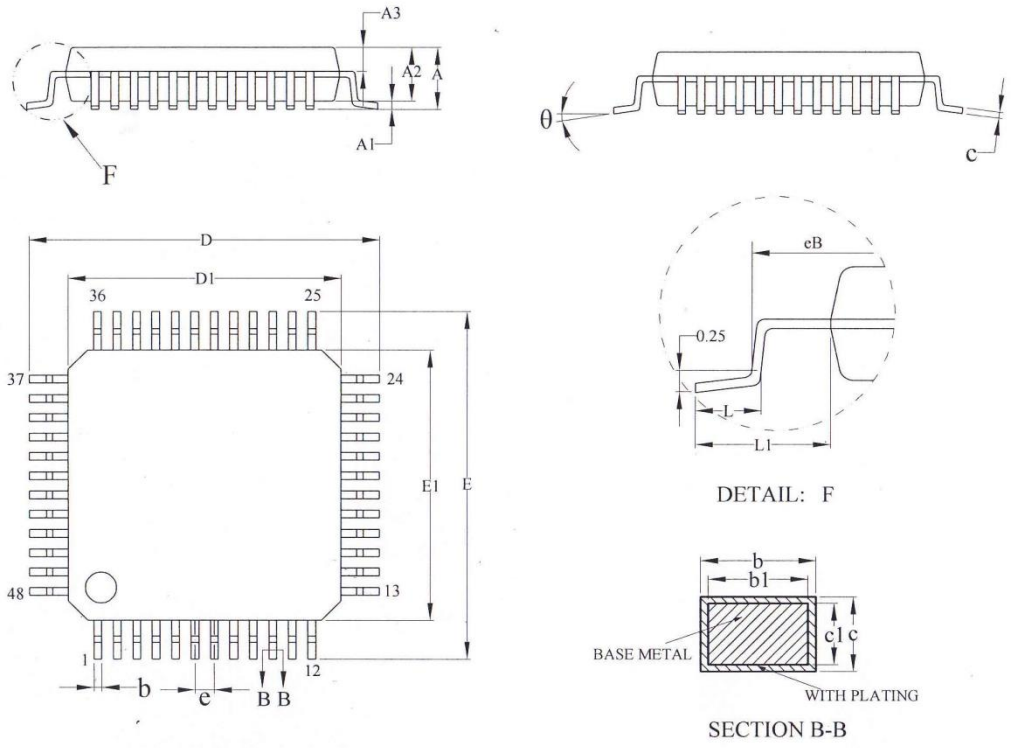
Grade	Millimeter		
	Minimum	Typical values	Maximum
A			1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.20
eB	15.05	-	15.35
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7 °



Map 29 LQFP64 , 64 Pin low profile quad flat package of FIG.

table 50 LQFP64 , 64 Low square cross section pin flat package data

Grade	Millimeter		
	Minimum	Typical values	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.25	-	11.45
E1	9.90	10.00	10.10
e	0.50BSC		
θ	0 °	-	7 °
L	0.45	-	0.75
L1	1.00REF		



Map 30LQFP48 , 48 Pin low profile quad flat package of FIG.

table 51LQFP48 , 48 Low square cross section pin flat package data

Grade	Millimeter		
	Minimum	Typical values	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.20
eB	8.10	-	8.25
e	0.50BSC		
L	0.40	-	0.65

L1	1.00REF		
k	0	-	7 °

6.2 Thermal Characteristics

The maximum junction temperature of the chip (T_J max) Must not exceed the table 6 Given range of values. The maximum junction temperature of the chip (T_J max) Expressed in degrees Celsius, the following formula can be used:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

among them:

- T_A max It is the maximum ambient temperature, with ° C He said,
- Θ_{JA} Is the junction to ambient thermal resistance of the package, with ° C / W Labeling,
- P_D max Yes P_{INT} max with $P_{I/O}$ max And (P_D max = P_{INT} max + $P_{I/O}$ max) ,
- P_{INT} max Yes I_{DD} with V_{DD} The product, in watts (Watt) Said, it is the maximum internal power dissipation of the chip.

$P_{I/O}$ max It is the maximum power consumption for all output pins:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}) ,$$

Consider applications I / O The actual low and high V_{OL} / I_{OL} with V_{OH} / I_{OH} .

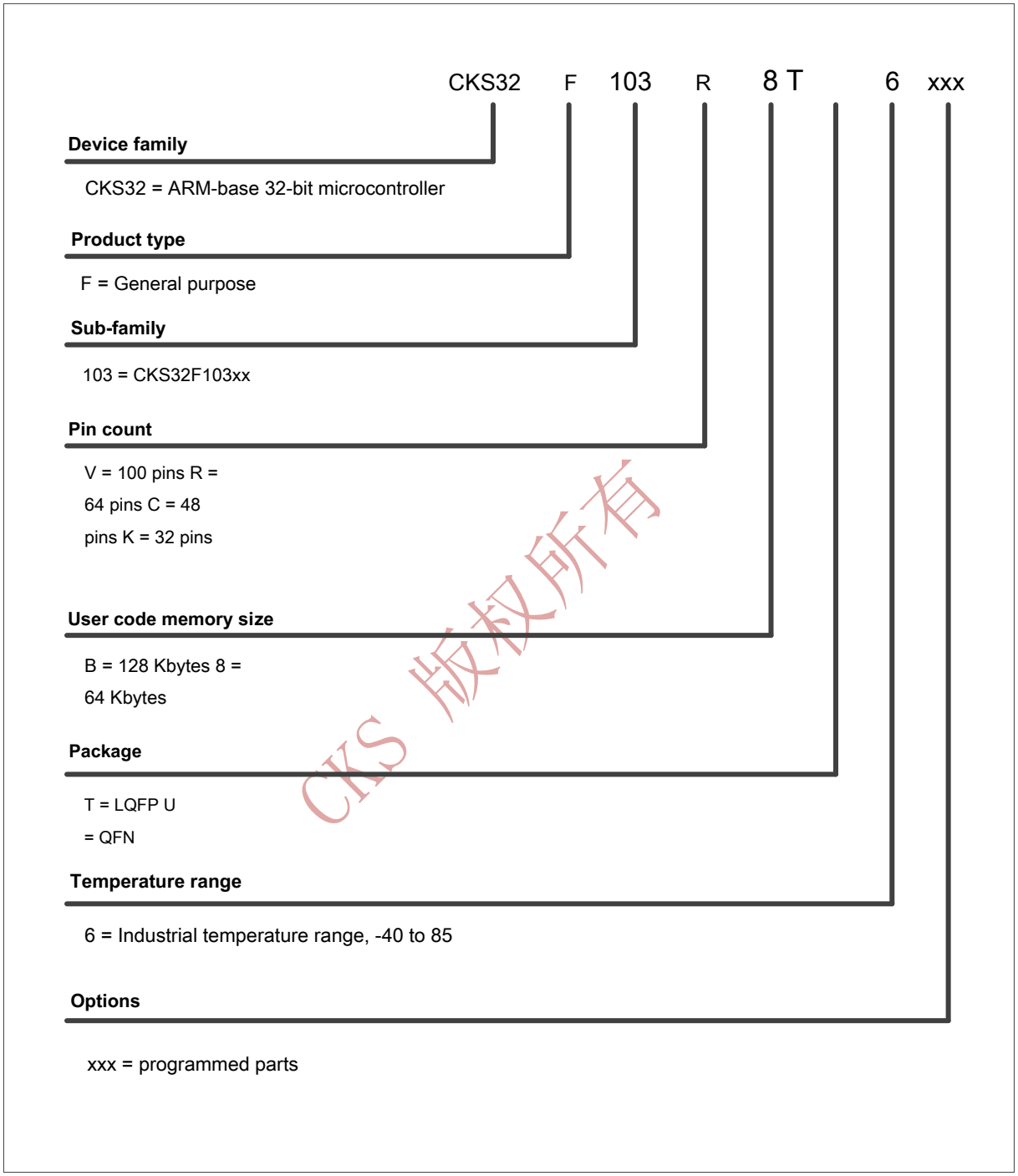
table 52 Thermal characteristics of the package

symbol	parameter	Value Unit	
Θ_{JA}	Junction the heat resistance of the environment –LQFP100 - 14 × 14mm / 0.5mm spacing	46	° C / W
	Junction the heat resistance of the environment –LQFP64 - 10 × 10mm / 0.5mm spacing	45	
	Junction the heat resistance of the environment –LQFP48 - 7 × 7mm / 0.5mm spacing	55	
	Junction the heat resistance of the environment –QFN36-6 × 6mm / 0.5mm spacing	18	

6.2.1. Reference Documents

JESD51-2 The integrated circuit thermal environmental condition - Natural convection (still air). See also www.jedec.org .

7. Model name



8. Version History

date	version	Modify part
2018.01.18	Initial draft	
2018.04.20	1.0	**Modify the map 3 The pin 80 And pin 81 The pin definitions; Table 14 Add clock 48MHz** Typical values of the conditions;
2018.08.11	1.1	**Add Table 15 Typical current consumption in the operation mode, the data processing code from the internal RAM Run; modify table 16 The clock 72MHz Typical values of the** conditions;
2018.10.10	1.2	**Modify table 18 in f_{LSE_ext} Maximum; modified table 26 in I_{DD} unit μA for mA ; Modify table 47 in V_{25} The minimum, typical and maximum values.**
2018.10.15	1.3	The device increases contrast / Ordering Information / model named chapters